ORDER NO. KMS0206640C1

F5

Service Manual

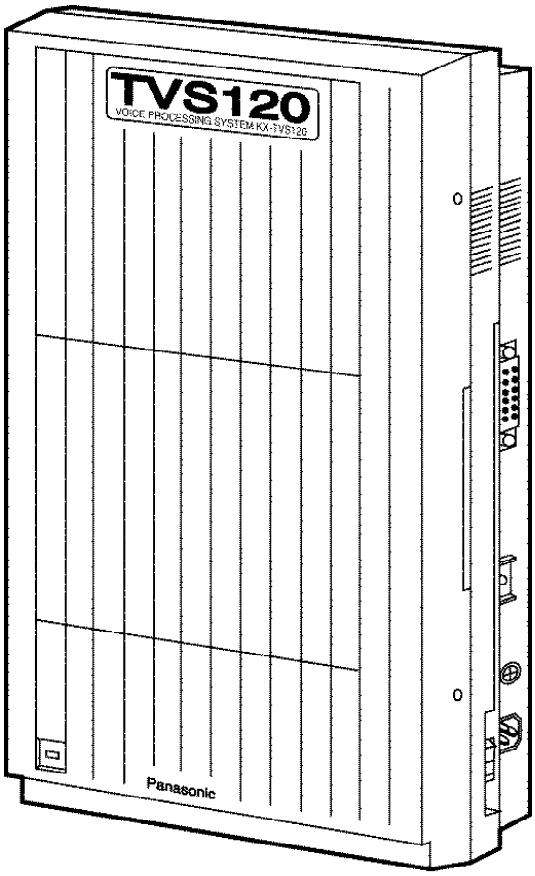
VOICE PROCESSING SYSTEM

KX-TVS120

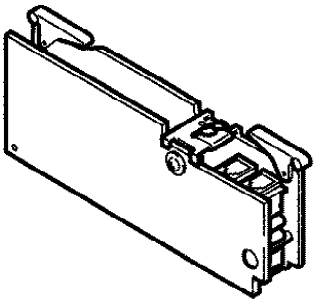
KX-TVS102

KX-TVS204

(for U.S.A.)



(KX-TVS120)



(KX-TVS102)

© 2002 Kyushu Matsushita Electric Co., Ltd. All rights reserved.
Unauthorized copying and distribution is a violation of law.

⚠ WARNING

This service information is designed for experienced repair technicians only and is not designed for use by the general public.
It does not contain warnings or cautions to advise non-technical individuals of potential dangers in attempting to service a product.
Products powered by electricity should be serviced or repaired only by experienced professional technicians. Any attempt to service or repair the product or products dealt with in this service information by anyone else could result in serious injury or death.

Panasonic

1. INTRODUCTION

1.1. CAUTION

When you mention the serial number, write down all 11 digits. The serial number may be found on the label affixed to the bottom of the unit.

1.2. SAFETY PRECAUTIONS

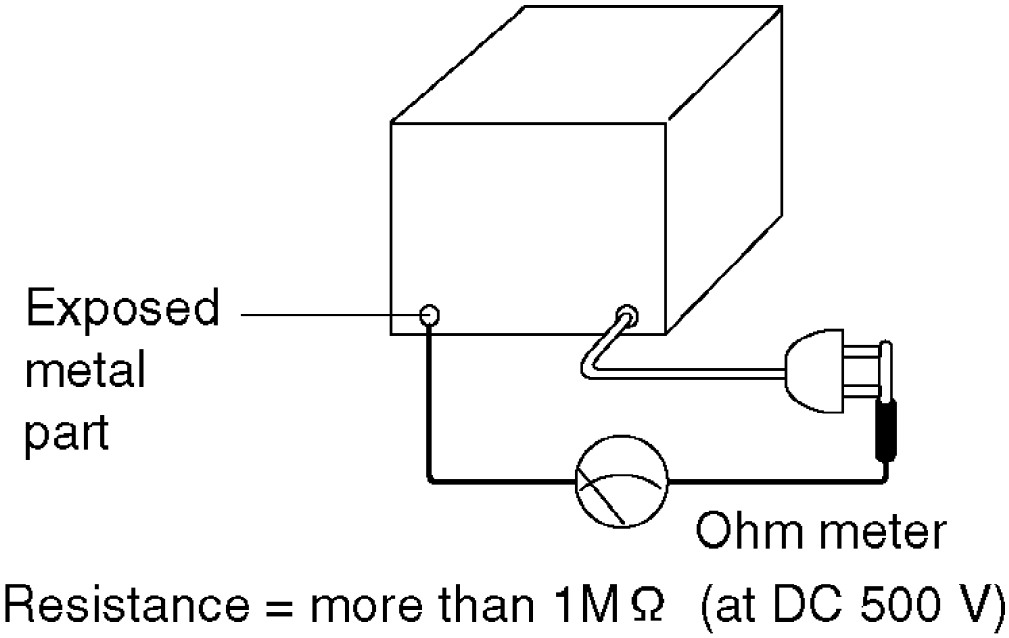
1. **Before servicing, unplug the power cord to prevent an electric shock.**
2. **When replacing parts, use only the manufacturer's recommended components for safety.**
3. **Check the condition of the power cord. Replace if wear or damage is evident.**
4. **After servicing, be sure to restore the lead dress, insulation barriers, insulation papers, shields, etc.**
5. **Before returning the serviced equipment to the customer, be sure to perform the following insulation resistance test to prevent the customer from being exposed to shock hazards.**

1.3. INSULATION RESISTANCE TEST

1. **Unplug the power cord and short the two prongs of the plug with a jumper wire.**
2. **Turn on the power switch.**
3. **Measure the resistance value with ohmmeter between the jumpered AC plug and each exposed metal cabinet part, such as screw threads, control shafts, handle brackets, etc.**

Note:
Some exposed parts may be isolated from the chassis by design. These will read infinity.

4. **If the measurement is outside the specified limits, there is a possibility of shock hazard. The equipment should be repaired and rechecked before it is returned to the customer.**



1.4. FOR SERVICE TECHNICIANS

ICs and LSIs are vulnerable to static electricity.

When repairing, the following precautions will help prevent recurring malfunctions.

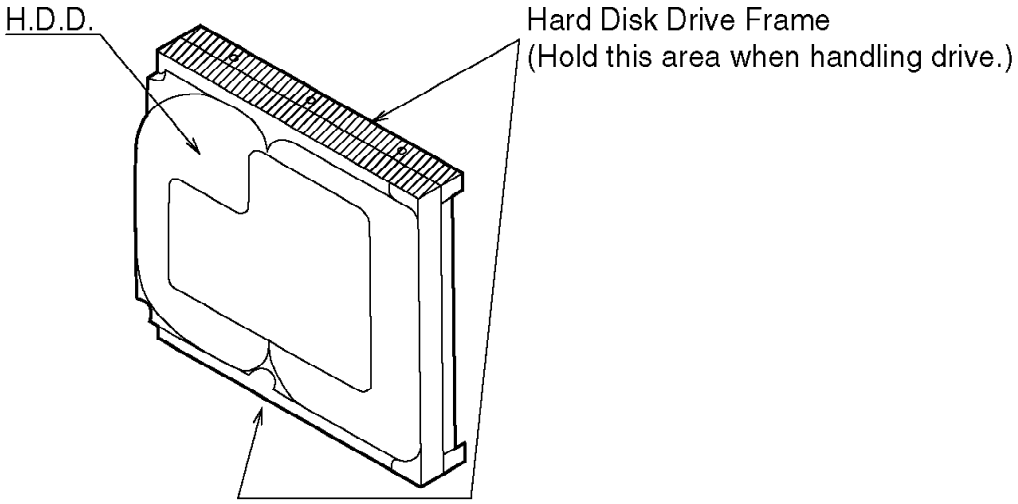
1. **Cover the plastic parts boxes with aluminum foil.**
2. **Ground the soldering irons.**
3. **Use a conductive mat on the worktable.**
4. **Do not touch IC or LSI pins with bare fingers.**
   Take special care when handling the Hard Disk Drive and KX-TVS120.

1.5. WARNING

CAUTION When Handling Hard Disk Drive!

1. **Beware of static electricity when handling the hard disk drive.**
2. **Do not touch circuit area.**
3. **Avoid hitting the drive with screwdriver when tightening screws.**
4. **Do not insert connector or tighten screws while pressing down on the surface of the hard disk drive. (Hold the hard disk drive frame when inserting connector or tightening screws.)**

5. The hard disk drive is extremely sensitive to impact; handle with care. Do not drop or jar.



1.6. BATTERY CAUTION

Danger of explosion if battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Discard used batteries according to following caution: Disposal of lithium batteries should be performed by permitted, professional disposal firms knowledgeable in state government federal and local hazardous materials and hazardous waste transportation and disposal requirements. Battery continues to have no transportation limitations as long as they are separated to prevent short circuits and packed in strong packaging.
Commercial firms that dispose of any quantity of lithium cells should have a mechanism in place to account for their ultimate disposition. This is a good practice for all types of commercial or industrial waste.
Recommend Type Number: CR2032(BATT)

1.7. CAUTION

The power socket wall outlet should be located near this equipment and be easily accessible.

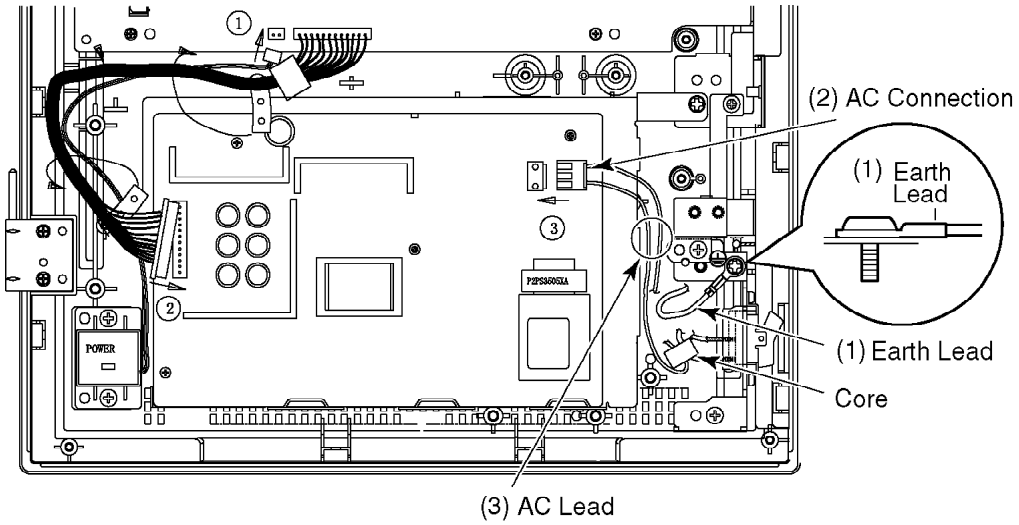
1.8. AC CAUTION

For safety, before closing the lower cabinet, please make sure of the following precautions.

1. The earth lead is fixed with the screw.

2. The AC connector is connected properly.

3. The AC lead is gotten though core.



2. SPECIFICATIONS

Port expansion Cards :		**KX-TVS102 (2 digital/analog port expansion card)(DSP/CO Card)(c KX-TVS204 (4 digital port expansion card)(DPT Interface Card)(fac installed card)(Original)**
Dialing Method :		**Touch tone/Pulse (10/20 pps)**
Flash Time :		**100/300/600/900 ms (programmable)**
CPC Detection :		**None/6.5/150/300/450/600 ms (programmable)**
Type of Line :		**Loop start minimum Loop Current: 20 mA Loop start minimum Line Voltage: 7 V DC Loop start minimum Ringing Voltage: 40 V AC**
Extension Numbering :		**2 to 5 digits (programmable)**
Pause Time :		**1 to 9 s (programmable)**
Message Waiting Lamp :		**Programmable Touch tone sequence**
Main CPU :		**16 bit microprocessor**
Hard Disk Capacity :		**Approximately 32 h**
Number of Mailboxes :		**Max. 64 (including System Manager and Message Manager mailbo**
Number of Messages :		**Max. 100 per mailbox (programmable)**
Personal Greeting Message Length :		**8 to 60 s (programmable)**
Message Retention Time :		**1 to 30 days or unlimited (programmable)**
Maximum Message Length :		**1 to 6 min., or unlimited length (programmable)**
Reports :		**Mailbox Assignment, COS (Class of Service) Assignment, System Service Report, Call Account Report, Port Usage Report, Disk Usa Report, Mailbox Usage Report, FAX call Report**
Connections	**Telephone Line :**	**In case of Inband, 2-conductor cable × 4 In case of DPT, 4-conductor cable with DPT interface × 3**
	Data Port :	**RS-232C interface port**
Operating Temperature :		**Please see Environmental Requirements**
Operating Relative Humidity :		**Please see Environmental Requirements**

Power Source :	**120V AC, 60 Hz**
Power Consumption :	**Approximately 25 W**
Dimensions (H × W × D) :	**470 × 335 × 110 mm** **(18-1/2" × 13-3/16" × 4-21/64")**
Mass (Weight) :	**Approximately 5.2 kg (11.46lb) (with 1 KX-TVS204{DPT Interface C installed at the factory)**

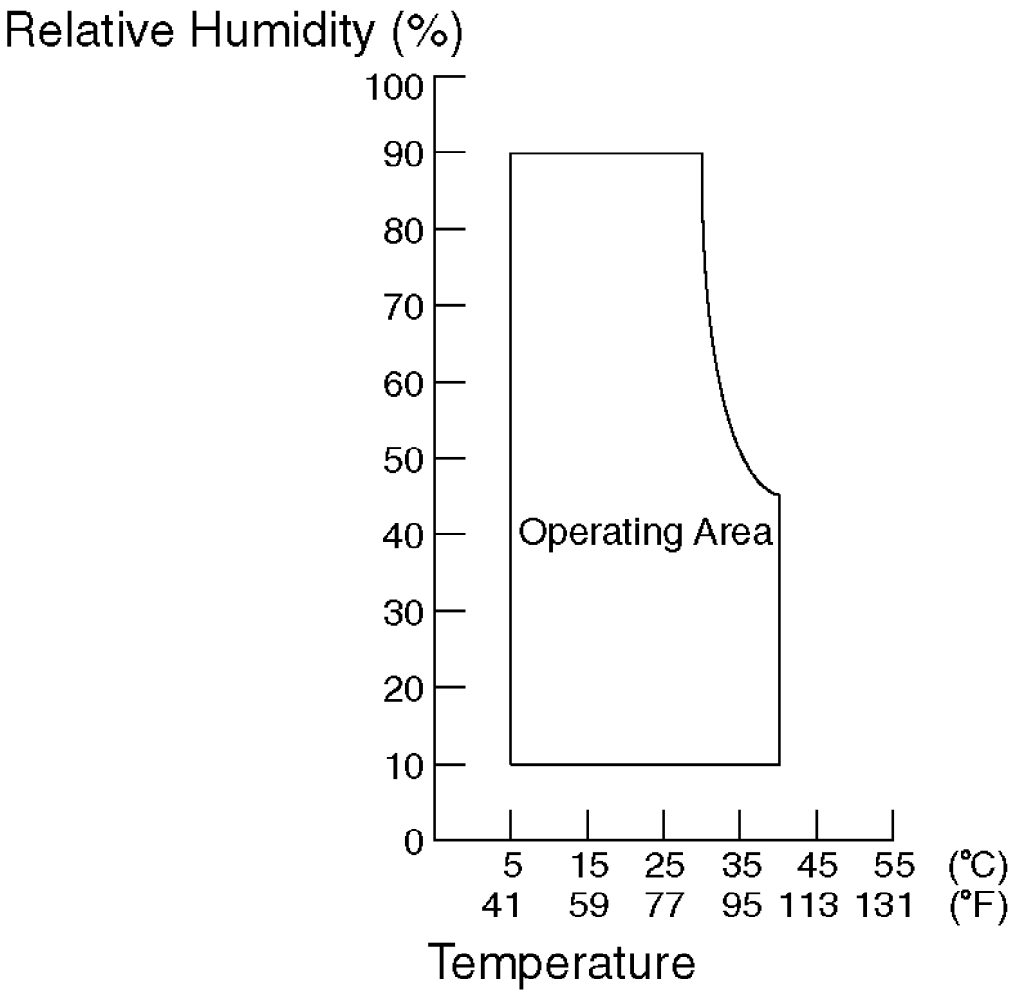
2.1. ENVIRONMENTAL REQUIREMENTS

The hard disk is sensitive to cold, heat, dryness, humidity, shock, vibration, and magnetic fields. Please observe the conditions specified below.

Hard Disk Drive Usage Environment

Operating Temperature :	**5°C to 40°C (41°F to 104°F)**
Operating Humidity :	**See Graph below.**
Shock :	**Under 5G**
Vibration :	**5 Hz to 22Hz : 0.0042 cm {0.020 inch} displacement; double amplit** **1 octave per minute.** **23 Hz 350 Hz : Under 0.5G**
Magnetic Field :	**DC: 0.6mT** **to 700 kHz: 0.7 μ T** **700 kHz to 1.5 MHz: 3 μ T**

Allowable Relative Humidity vs. Temperature



3. OVER VIEW

This chapter describes the hardware overview of the Voice Processing System (VPS).

3.1. SYSTEM OUTLINE

The Panasonic Voice Processing System (VPS) is a voice prompted, menu-driven system which provides fully automated call transfer (to an extension or mailbox), and voice message receiving and delivery service. Even first time users can easily reach their desired extension or mailbox by following step-by-step voice instructions.
The VPS works with a PBX as an extension. It can be expanded to handle up to 6 simultaneous calls and store up to 32 hours of voice data.
The VPS attends to incoming calls, then transfers those calls to the respective extensions. When owners of extensions cannot answer the call, the mailboxes in the system take messages for them. Owners of the mailboxes can record personal greeting messages with their own voice for callers who enter the mailbox to leave messages.
The VPS has up to 62 personal mailboxes for subscribers and two special function mailboxes for the System Manager and Message Manager.
The VPS can be used by any caller, and by subscribers (Mailbox Owner) in your company. Even if the user is away from the office, VPS can be used with any touch tone telephone.

Even callers using a rotary telephone can leave messages or be connected with the operator. The VPS provides the following incoming call services to callers.

3.1.1. AUTOMATED ATTENDANT (A.A.) SERVICE

The automated Attendant works as a receptionist would by answering incoming calls without human intervention.
The Automated Attendant plays a list of options (calling extension, calling operator, Department Dialing, Dialing by Name) to a caller with a voice prompt. When an option has been selected, the Automated Attendant responds to the command by either routing the caller to an extension or the operator. The Automated Attendant will even respond if the extension is busy or if there is no answer.
One option is to let the caller leave a message in a mail box.

3.1.2. VOICE MAIL (V.M.) SERVICE

Voice Mail is a voice message receiving and delivery service which allows subscribers (the owner of a personal mailbox) to receive messages in their mail box whether they are out of the office, on the line, or just unavailable to answer the call.
Any caller can leave a message in a subscriber's mailbox. The subscriber can listen, transfer, and deliver recorded messages at any time from anywhere in the world.

3.1.3. INTERVIEW SERVICE

You can set up a questionnaire mailbox with as many as 10 questions, and obtain specific information from customers calling into the system. Between each recorded question, the VPS collects a reply from the caller and stores it in a mailbox.
This service is ideal for gathering any data from product orders to requests for repairs.

3.1.4. CUSTOM SERVICE

The Custom Service capability optimizes the application of the VPS to meet your business needs. Your callers can access the services or people they need by pressing a single digit on their telephone keypad.

3.2. SYSTEM PROGRAMMING

This system can be programmed either by a data terminal (VT100, compatibles, or other ASCII terminals) through the System Administrator Interface or by telephone (touch tone telephone) through the System Manager mailbox.

3.2.1. TERMINAL BASED PROGRAMMING

After system installation, it is recommended that you perform "Quick Setup" first.

<Quick Setup>
Provides a fast way of setting up the VPS for basic Voice Mail or Automated Attendant service. This includes mailbox creation, incoming call service assignment for all ports, time setting and several other programming items which must be done initially to start the VPS operation.

<PBX Integration>
In its initial state, the KX-TVS120 provides 4 ports with KX-TVS204(DPT Interface Card),and 6 ports of DPT Integration by installing KX-TVS102(DSP/CO Card) option port . Typically, each VPS port is connected to an extension port of the PBX.
Between PBX's, the VPS exchanges a request to a counterpart or status for itself mutually, then offers a quick and useful service. The VPS works well with all Panasonic KX-T series PBX's and can be programmed to work with most other manufacturer's PBX's that fully support single line telephone interfaces.
However, because the VPS operation depends on the capabilities and features provided by the PBX, its performance will vary when connected to different PBX's. In system program, Integration Parameter with a PBX should be installed to achieve quicker and more useful service.

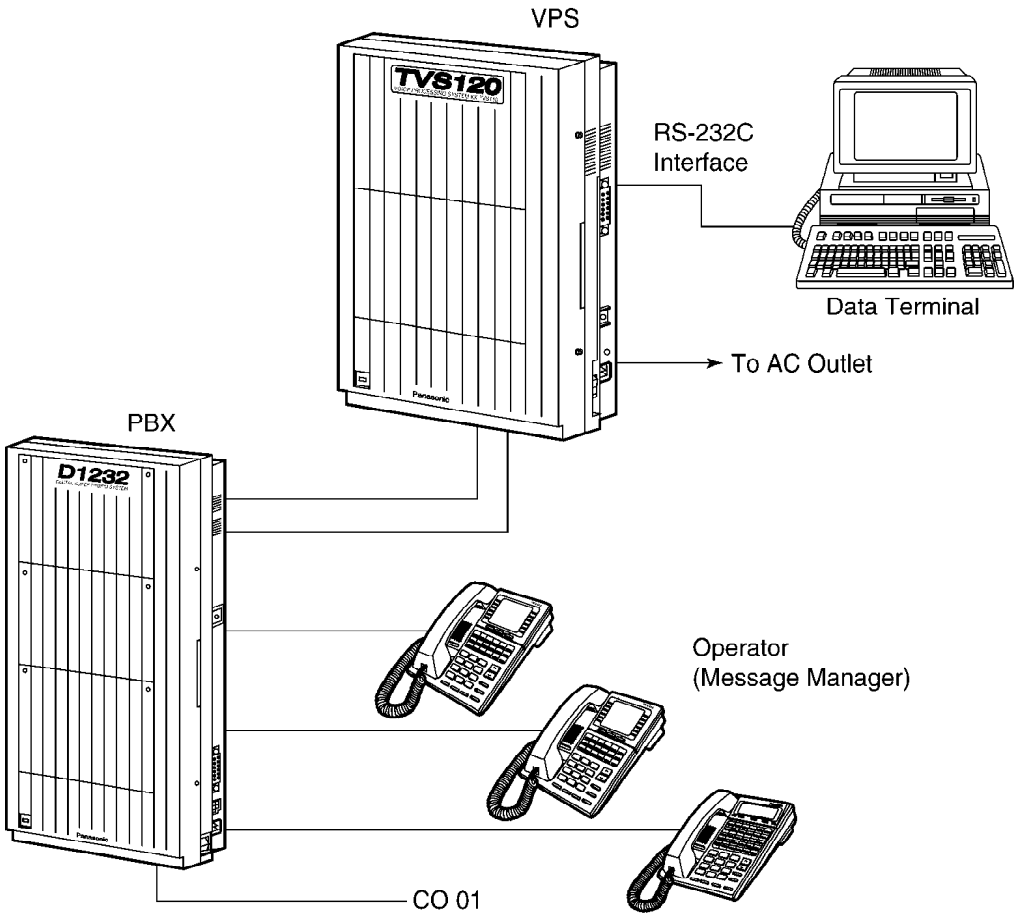
3.2.2. TELEPHONE BASED PROGRAMMING

During daily operation, the person specified as the System Manager can create and/or delete mailboxes, and change Class of Service parameters.

3.3. SYSTEM CONFIGURATIONS

The most common configuration of the VPS is behind a PBX. The VPS ports are connected to PBX extension ports.

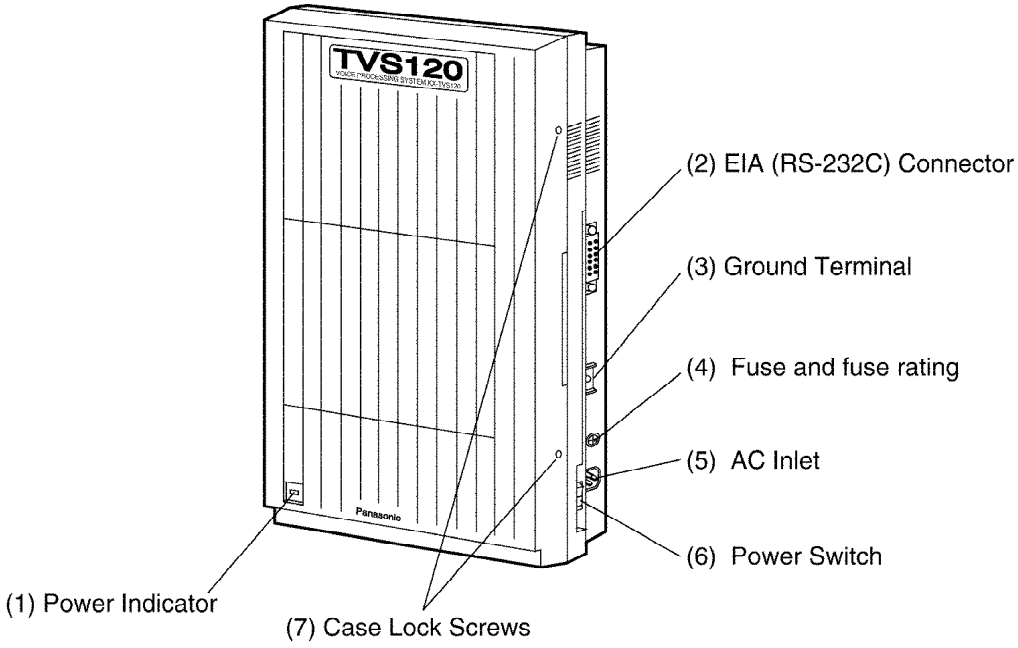
Typical Configurations



3.4. SYSTEM COMPONENTS

3.4.1. OUTSIDE EQUIPMENT

Cabinet Outside View and Equipment Location



(1) Power Indicator
Power Indicator indicates VPS status. When you turn on the power switch, the power indicator turns on. During this period, the VPS executes self diagnostics. When the self diagnostics finishes normally, this indicator starts the blinking sequence. During this period, the VPS executes the system initialization. When this initialization finishes normally, the indicator lights on again, and the VPS starts the incoming service. When the VPS detects any error on system, the Indicator informs the type of error by using a specific blinking sequence.

(2) EIA (RS-232C) Connector
The VPS allows to communicate with a Data Terminal or with any standard ASCII Terminal for system programming. The terminal is connected to the VPS using an RS-232C cross cable. Attach the 25-pin connector to the jack marked "RS-232C" on VPS.

(3) Ground Terminal
Ground Terminal is an earth terminal.
Tie the ground line to the Ground Terminal marked "GROUND" on the VPS.

(4) Fuse and fuse rating
This fuse is a safety part for AC power line. In order to use the VPS safely, it is required to use a regulated fuse indicated on the label.

(5) AC Inlet
AC inlet is an input connector of AC power source. Attach AC power code to AC Inlet marked "AC IN" on the VPS.

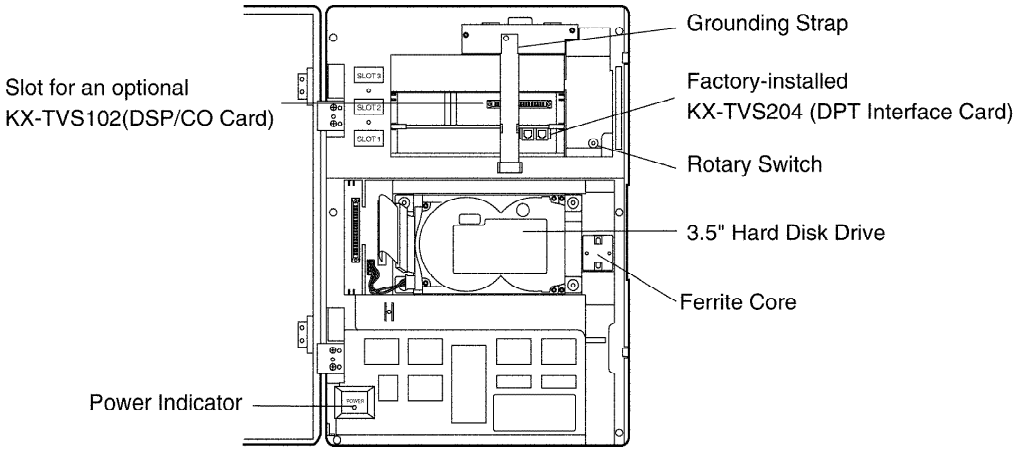
(6) Power Switch
Turn the power switch on the side of marked "ON", then AC Power is supplied to the VPS.
Turn the power switch on the side of marked "OFF", then supply of AC Power is cut.

(7) Case Lock Screws
The VPS has two case lock screws to open the front cover.

3.4.2. INSIDE COMPONENTS

Inside of the VPS is covered by two pieces cabinet. These two cabinets are fixed to the base cabinet with two and four screws.

Inside View and Components Location



(1) 3.5" Hard Disk Drive (HDD)

The Hard Disk Drive (HDD) is installed Proprietary System Program and System Prompt. All the recorded messages from callers are stored in the HDD. The HDD is connected to Main Board using a 40 pin flat cable and 4 pin power cable.

(2) Grounding Strap

This Grounding Strap is an earth plate. To protect the printed circuit board from static electricity, first discharge any body static by touching the grounding Strap.

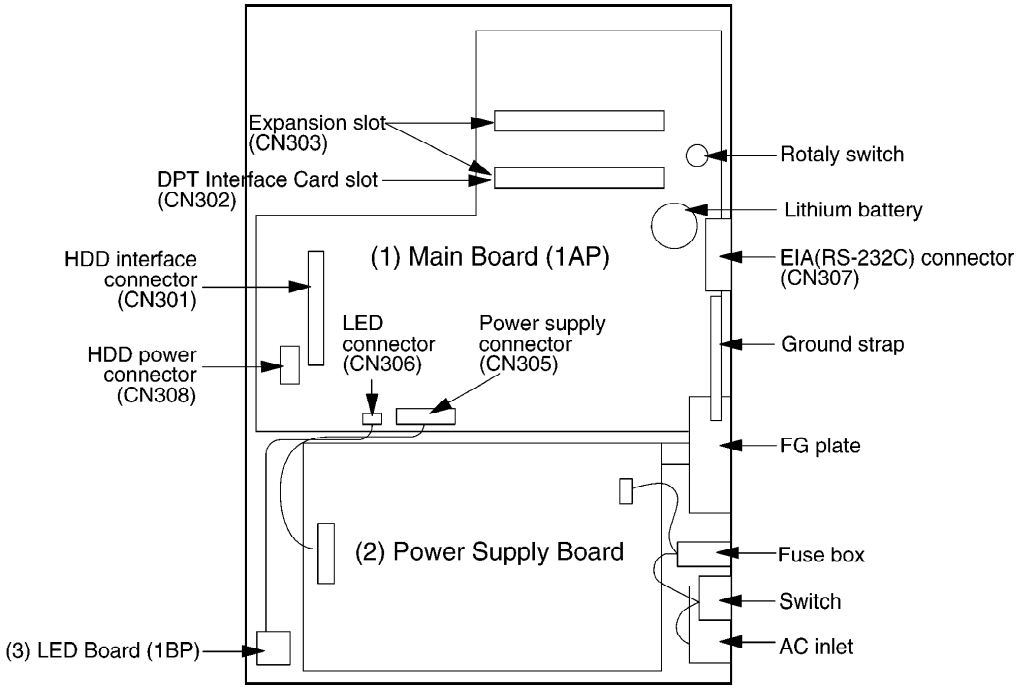
(3) Rotary Switch

The Rotary Switch Provides additional function as follows. The status of this switch is checked only once after power-up. The additional functions are effective when you turn on the power after the switch changing.

Position	Additional Function
0	Normal setting.
1	Initializes RS-232C parameters. RS-232C default parameters: 9,600, N, 8, 1
2*	Auto Configuration is automatically completed and all ports are set for Automat Attendant service.
3*	Auto Configuration is automatically completed and all ports are set for Voice Ma service.
4	Reserved
5	Initializes the VPS. Clears all voice data (except User 1 and User 2 prompts) and returns all system parameters to the default setting.
6	Test Mode (Hard Disk Drive Read/Write Test)
7	Reserved
8	Initializes the VPS. Clears all voice data and returns all system parameters to the default setting. **Caution:** User 1 and User 2 Prompts will be erased!
9	Reserved

*** For Panasonic KX-T series telephone system with DPT Integration.**

3.4.3. BASIC COMPONENTS



(1) Main Board (1AP)

The Main Board is the central processing unit of the VPS. When power is on, the microprocessor (IC301) on the Main Board runs on the ROM (IC306) based program, and

executes the system initialize, self diagnostics and then an application program loading from HDD to system RAM on the Main Board. After the program loading, Main Board starts the incoming call service. The Main Board allows to control the RS-232C interface and the real time clock device with back up battery. The Main Board has 9 interface connectors as follows.
CN301 = HDD interface connector (40pin)
CN302 = DPT Interface Card slot (KX-TVS204)(Original) /Expansion slot (KX-TVS102)(DSP/CO Card)(Option) (50pin)
CN303 = Expansion slot (KX-TVS102)(DSP/CO Card)(Option) (50pin)
CN305 = Power supply connector, DC power supply from Power Supply Board (8pin)
CN306 = LED connector, Power Indicator (LED) interface (2pin)
CN307 = EIA(RS-232C) connector, RS-232C interface (25pin)
CN308 = HDD power connector,HDD Power supply (4pin)

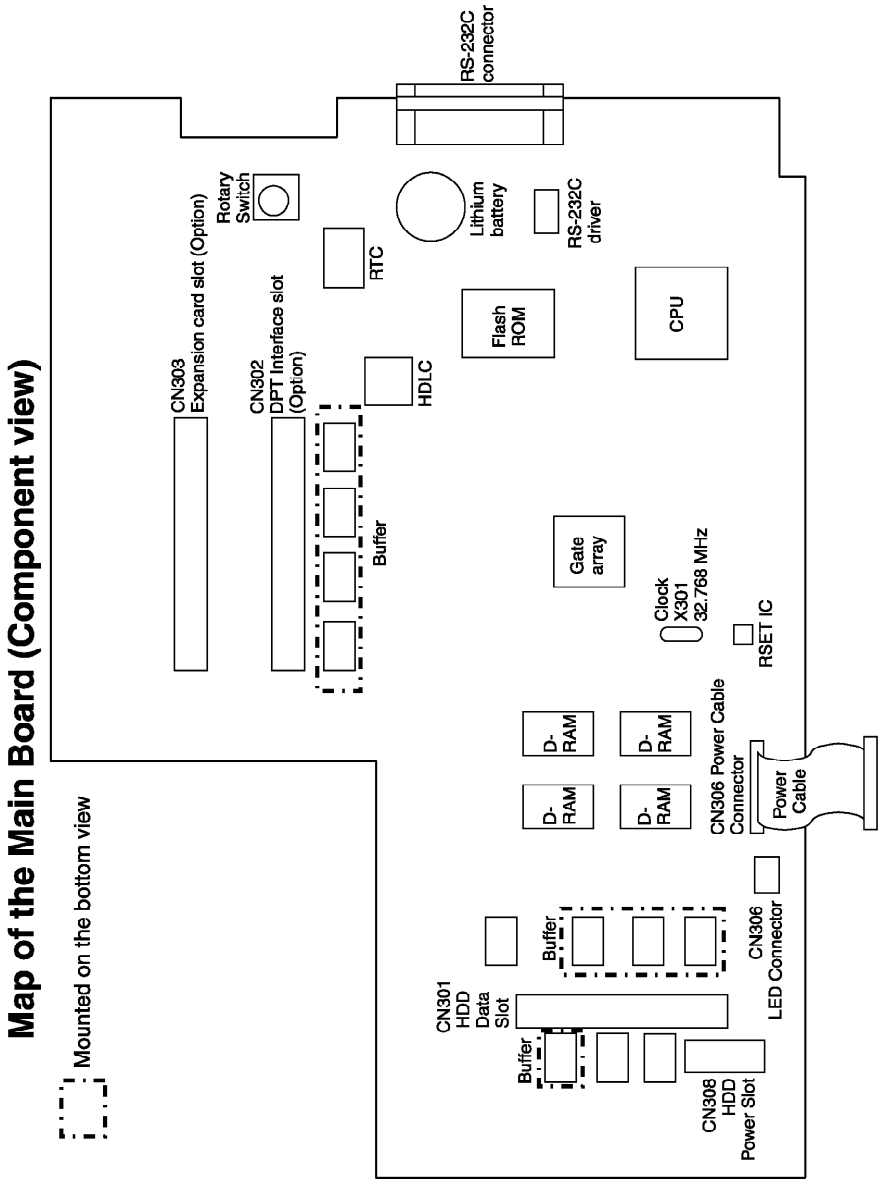
(2) Power Supply Board
The AC power source inputs from AC inlet.
Power Source inputted from AC Transformer is rectified in Power Supply Board, and then changed to DC +12V, to DC +5V and to DC-5V. Functions of Power Supply Board is as follows.

- **DC5V, +12V generation.**
- **DC+5V back up by using large capacity capacitor.**
- **Power down detection.**
- **DC shut down control in case of abnormal condition of the voltage, current and temperature.**

This Power Supply Board has a variable resister (VR101) for +5V DC voltage adjustment.
DC power source generated in Power logic is supplied to Main Board via CN101.

(3) LED Board (1BP)
LED Board is connected to Main Board via CN306 and its ON/OFF states are controlled by the Main Board.

3.4.3.1. EXAMPLE OF MAIN BOATD



Explanation of Main board Parts
(1) Main Board IC or parts

1. CPU : TMP68301 16M 100pin QFP

2. Flash ROM : 4Mbit Flash Memory × 1

3. Gate Array : 120pin QFP

4. DRAM : 4Mbit × 4

5. HDLC : MITEL MT8952 28pin

6. RTC : OKI M6242B

7. RS-232C driver : +5V power type

8. Lithium Buttery : CR2354

9. Buffer ICs : LS244 or LS245

10. Clock(X301) : 32.768MHz

11. RESET IC : MITSUMI T520C

(2) factory installed Slots(Original)

1. DPT Interface Card(KX-TVS204)Slot : 50pin × 1

2. HDD Data Slot : IDE Interface 40pin × 1

(3) Expansion Slots(Option)

1. Expansion Card Slots for KX-TVS102(DSP/CO Card) : 50pin × 2
KXTVS120 can contain TVS102(DSP/CO Card) in Slot 1(CN302) by removing DTP interface card(KX-TVS204) of slots 2(CN303)

(4) Connector

1. HDD Power Connector : IDE 4pin × 1

2. RS-232C Connector: 25pin D-sub

3. Power Cable Connector : Connect to Power Supply Board

4. LED connector : Connect to LED PCB

(5) Switch

1. Rotary Switch : 10pattern

Main Board

(1)CPU (IC301)
KX-TVS120 uses Motoroller MC68302CPU as main CPU. It is a QFP package goods of 100pin with 16.384MHz of frequency for operation. This CPU controls totally all functions of KX-TVS120.

(2)Flash ROM (IC306)
KX-TVS120 uses Fujitsu Nor type Flash Memory with 4Mbit as main memory. This Flash Memory

contains software for system program boot and for production test and the latest system program is downloaded from HDD when starting up the system.

(3)Gate Array (IC302)
KX-TVS120 has a specific Gate Array with 120pin QFP. This Gate Array has functions for system control, voice DMA control, HDD interface and DRAM control.

(4)DRAM (IC304,IC305,IC307,IC309)
KX-TVS120 contains four DRAMs consisting of 512kbit × 8 = 4Mbit.KX-TVS120 uses this DRAM memory area as working memory for application, voice buffer for transmitting voice data DMA.

(5)HDLC (IC303)
KX-TVS120 contains one MITEL MT8952, HDLC controller. This controller enables DPT data link with PBX of Panasonic TD series.

(6)RTC (IC308)
KX-TVS120 contains one OKI M6242B, real time clock IC. With this real time clock IC, current time data can be taken out and time stamp of recorded messages or other operations controlled by time can be started up.

(7)RS-232C driver (IC311)
KX-TVS120 contains one RS-232C IC for driver receiver. One RS-232C port consists of this IC.

(8)Lithium Buttery (BAT301)
KX-TVS120 contains one lithium battery for back-up of RTC clock data. With this battery, set up current time data can be backed up if the main power supply of the system is turned OFF.

(9)Buffer ICs (IC312,IC313,IC314,IC315,IC316,IC317,IC318,IC319,IC320)
KX-TVS120 equips itself with TTL buffer at expansion slot, and at input and output points of signal lines such as HDD interface. With this buffer, sending and receiving signals with the card contained in each expansion slot is assisted.

(10)Clock (X301)
KX-TVS120 has crystal oscillator with 32.768MHz as the source of system clock.

(11)RESET IC (IC310)
KX-TVS120 contains one MITSUMI Reset IC(T520C). With this IC, the whole system is reset forcefully when the power supply starts up or is turned OFF.

factory installed Slots(Original)

(1)Expansion Card slot for KX-TVS204(DPT Interface Card) or KX-TVS102(DSP/CO Card) (CN302)
KX-TVS120 has one slot connectors as Expansion Card slot (Original). This card slot connector can contain KX-TVS204(DPT Interface Card) in Slot 1 (CN302). This card slot comnector also can contain KX-TVS102 (DSP/CO Card) by removing KX-TVS204 (DPT Interface Card).

(2)HDD Data Slot (CN301)
KX-TVS120 has one IDE interface to connect with 3.5" HDD. This slot is connected with a flat cable with 40pin and used for transmitting IDE interface data.

Expansion Slots(Option)

(1)Expansion Card Slots for KX-TVS102(DSP/CO Card) (CN303)
KX-TVS120 has two slot connectors as expansion card slot(Option). This card slot connector can contain KX-TVS102(DSP/CO Card) only.

Connector

(1)HDD Power Connector(CN308)
KX-TVS120 contains one connector for power supply to HDD as IDE interface to connect with 3.5" HDD.

(2)RS-232C (CN313)
KX-TVS120 contains one D-sub connector with 25pin for RS-232C. With this connector, maintenance by PC and various set-ups can be done.

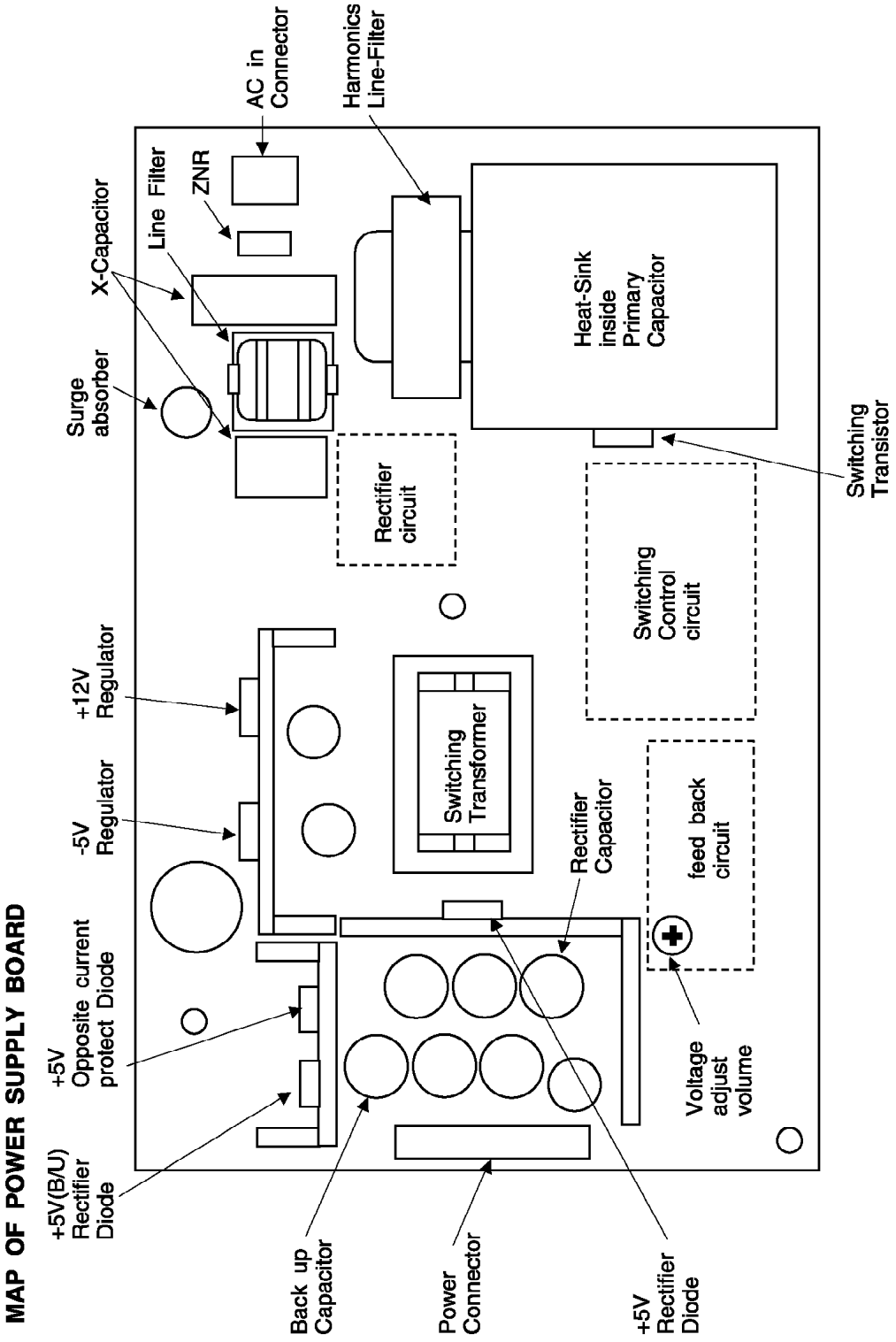
(3)POWER Cable (CN311)
KX-TVS120 has POWER Cable with 12pin to supply power from the power unit.

(4)LED Cable (CN312)
KX-TVS120 has one connector to connect with LED board with function of power ON and OFF and system alarm display.

Switch

(1)Rotary Switch (SW301)
KX-TVS120 contains one Rotary switch with 10 patterns that can instruct specific operations. The specific operations allocated to each switch pattern can be instructed to KX-TVS120 by restarting the power supply after setting this Rotary switch.

3.4.3.2. EXAMPLE OF POWER SUPPLY BOARD



Explanation of Power Supply Board Parts

(1) Power Supply Board parts or Circuit or Connector

1. ZNR
2. Heat-Sink
3. Primary Capacitor
4. Switching Transistor
5. Harmonics Line-Filter
6. X-Capacitor
7. Line-Filter
8. Surge absorber
9. Rectifier Circuit
10. Switching Control circuit
11. Switching Transformer
12. feed back circuit
13. Voltage adjust volume
14. Rectifier Capacitor
15. Rectifier Diode
16. Regulator
17. Back Up Capacitor
18. Power Connector

Power Supply Board parts, Circuit or Connector

(1)ZNR (ZNR1)
This ZNR prevents over voltage applied inside by being short mode when over voltage is input. It also stops the continuation of phenomenon by cutting fuse at the time of short mode.

(2)Heat-Sink
This Heat Sink has both functions for heat sink of switching transistor and explosion protection of primary condenser.

(3)Primary Capacitor (C5)
This Capacitor rectifies AC input voltage in combination with Rectifier Diode.

(4)Switching Transistor (Q1)
This Transistor is used to control the secondary voltage by re-switching DC voltage after rectifying AC.

(5)Harmonics Line-Filter (L2)
This Harmonics Line-Filter is to remove harmonics noise of power supply.

(6)X-Capacitor (C1,C2)
This X-Capacitor is to remove noise among Live-Neutrals of AC power supply.

(7)Line-Filter (L1)
This Line-Filter is to remove noise among Live-Neutrals of AC power supply.

(8)Surge absorber (SA1)
This Surge absorber is to remove surge noise input from AC power supply.

(9)Rectifier Circuit
This Rectifier circuit rectifies AC input voltage in combination with Primary Capacitor.

(10)Switching Control circuit
With this circuit, ON-OFF of Switching Transistor is controlled.

(11)Switching Transformer (T1)
This Transformer transmits switched power to the secondary side keeping isolation between the primary and the secondary.

(12)Feed back circuit
With this feed back circuit, voltage at the secondary side is observed and switching timing at the primary side is adjusted.

(13)Voltage adjust volume (VR101)
With this volume, slight adjustment of voltage within the secondary voltage + 5V is available.

(14)Rectifier Capacitor (C101,C103,C104,C105,C106)
This Rectifier Capacitor rectifies the switching waveform in combination with Rectifier Diode.

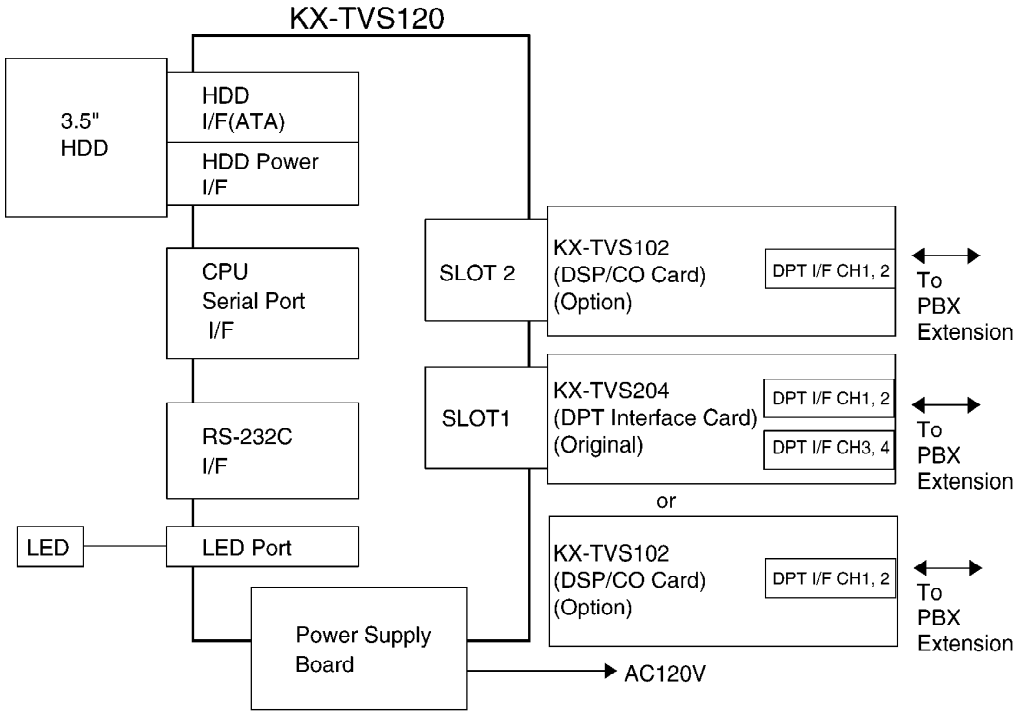
(15)Rectifier Diode (D101,D102,D103,D104,D106,D107)
This Rectifier Diode rectifies the switching waveform in combination with the Rectifier Capacitor.

(16)Regulator (IC101,IC202)
With this Regulator, +12V and -5V are supplied continuously.

(17)Back Up Capacitor (C201,C202,C203,C102)
This Back Up Capacitor maintains the back up voltage of +5V and +12v at the time of temporary failure.

(18)Power Connector (CN101)
With this Connector, power voltage is supplied to the main board.

3.4.4. HARDWARE ARCHITECTURE OUTLINE



Functions of each hardware block are explained by giving an example of the process from guidance play back to message recording by Voice Mail Service.

(1)Bell arrival(When KX-TVS102{DSP/CO Card})
Line interface has a function to detect the bell signal inputted from Tel Jack. The 16 bit CPU monitors this bell arrival through the Line Control Port periodically. When the 16 bit CPU

detects the bell arrival, the CPU makes the line condition into an off-hook state through the line control port.

(2)Guidance Play back(When KX-TVS102{DSP/CO Card},KX-TVS204{DPT Interface Card})
At the same time the CPU transfers system prompt data stored in the HDD in advance from HDD to a voice buffer area in the system memory. (This system prompt data is compressed in half by ADPCM algorithm)
The CPU programs the Voice Transfer logic to the play back mode. In addition, the CPU writes the play back command into FIFO on the DSP G/A. DSP monitors this FIFO periodically. If DSP receives a playback command by FIFO monitoring, DSP starts to execute ADPCM play back. In ADPCM play back the following processes are executed.
System prompt data, transferred from system memory by the voice data transfer logic, is encoded to digital voice data. In case of KX-TVS102(DSP/CO Card), then output to CODEC.The CODEC converts digital voice data to analog voice data, and outputs to the line interface . In case of KX-TVS204(DPT Interface Card) ,then output to DPT I/F. In ADPCM play back mode, the DTMF detecting function is always activated and checks reception of the DTMF code by DSP.

(3)Message Recording
When DSP detects a DTMF code represented recording, it writes the DTMF code into FIFO. CPU monitors this FIFO periodically. The CPU receives DTMF code represented recording messages intermittently, then the CPU programs Voice Data Transfer logic to Recording mode. The Message recording command is written into FIFO on the DSP card. DSP receives message recording command intermittently, DSP starts to execute ADPCM recording. In ADPCM recording, the following processes are executed. In case of KX-TVS102(DSP/CO Card), voice data input from the line interface is converted to digital voice data by CODEC DSP receives digital voice data from CODEC and executes the voice data compression based on ADPCM algorithm. In case of KX-TVS204(DPT Interface Card),voice data input from DPT interface is converted to PCM data by CODEC DSP receives digital voice data from CODEC and executes the voice data compression based on ADPCM algorithm. DSP outputs the compressed data to Voice data transfer logic. Voice data transfer logic transmits the compressed data from DSP to system memory. Data transferred to system memory is stored in HDD by the CPU. In ADPCM recording mode, DTMF detecting function, Tone detecting function, and VOX (silence) detecting function are always activated by DSP. The result of this detection is written into FIFO by DSP periodically.

(4)End of Message Recording disposition
The CPU receives these detection results via FIFO, then detects the recording termination. (For example the conditions of termination are to receive the DTMF code representing recording finish, detect a Busy Tone or a detected silence situation more than a regulated period, etc.)
When the CPU detects a recording, it terminates the recording disposition then shifts over to the next step, guidance play back disposition.

(5)The functions of the module
The functions of the module are as follows.

- HDD
  to store the voice data, and the system program.
- System memory
  to store voice data temporarily, to execute the system program.
- Voice Data Transfer logic
  to control the transfer of voice data between DSP to/from system memory.
- DSP voice compression/decompression (using ADPCM Algorithm).
  to detect and generate DTMF.
  to detect Tone and generate Beep Tone.
  to detect VOX (silence).
  to adjust recording level. (Automatic Recording Level Control)
- Codec
  Analog to/from digital conversion of the voice data.
- CPU
  Controls all of the system.

4. INSTALLATION

4.1. INSTALLATION REQUIREMENTS

The VPS installation involves

- Mounting the VPS.
- Connecting PBX extensions to the VPS ports.
- Connecting a Data Terminal (VT or ASCII)
- Connecting Power to the Cabinet.
- System Programming (‘ Refer to Installation Manual)

Installation personnel should be familiar with the data format and change procedures of the PBX. For further explanation, refer to the "Installation Manual".

4.1.1. SITE REQUIREMENTS

Install the VPS cabinet in a dust free location. Keep it separated from other equipment that may produce heat or generate strong magnetic fields. If space permits, install the VPS in a telephone equipment room.

4.1.2. AC POWER REQUIREMENT

It is best to power the system from a dedicated, separate circuit. If this is not possible, make sure the circuit is free of large motorized equipment, such as copy machines, and that it is

protected by a fuse or circuit breaker.
Make sure the power receptacle is grounded and within five feet of the cabinet.

4.1.3. OTHER REQUIRED EQUIPMENT

Each VPS port is connected via a modular line cord to a standard modular telephone jack connected to a PBX extension. Each line cord must be of sufficient length to reach between the VPS and PBX without undue stretching or tension. Keep it separated from other cords that may generate strong electric magnetic wave.
A data terminal, used for system programming, must be available at the customer site. In addition, one RS-232C cross cable is required to connect the terminal to the VPS.

The following is a list of required equipment.

Table 1-1, Installation required equipment.

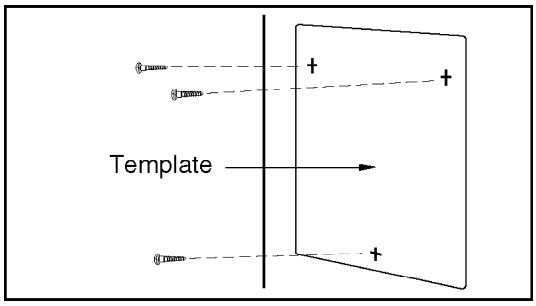
Modular line Cord (male-male)	**4 wire**	**1 cord/2 port (when connecting Panasonic KX-TD Series PBX extension)**
	2 wire	**1 cord/1 port (when connecting other type PBX extension)**
Data Terminal (VT or ASCII)	**1**	
RS-232C Cross Cable	**1**	
Screw Driver	**1**	
Drill	**1**	

4.2. MOUNTING THE VPS

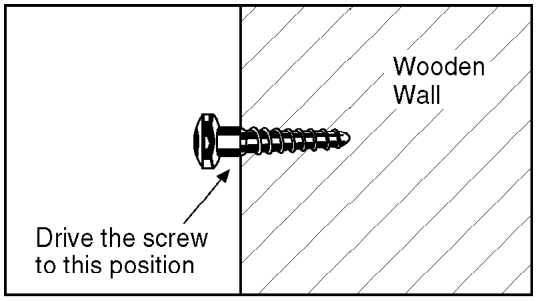
Mounting the VPS on the Wall
The wall where the VPS is to be mounted must be able to support the weight of the VPS. If screws other than the ones supplied are used, use the same-sized diameter screws as the enclosed ones.

To Mount on a Wooden Wall:

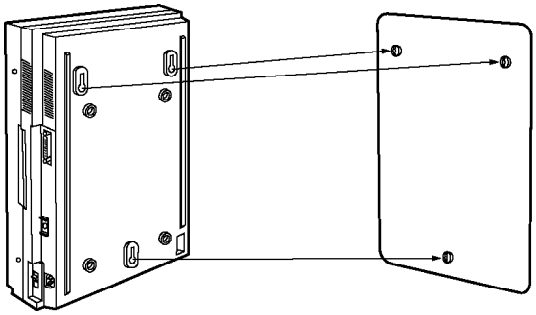
1. **Place the template (included) on the wall to mark the 3 screw positions.**



2. Install the 3 screws into the wall.



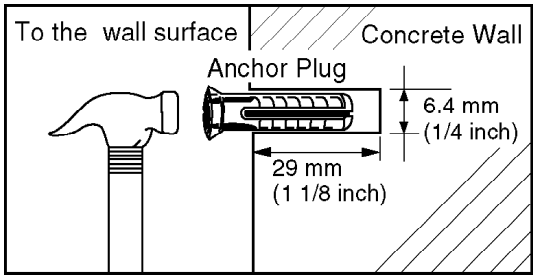
3. Hook the unit on the screw heads.



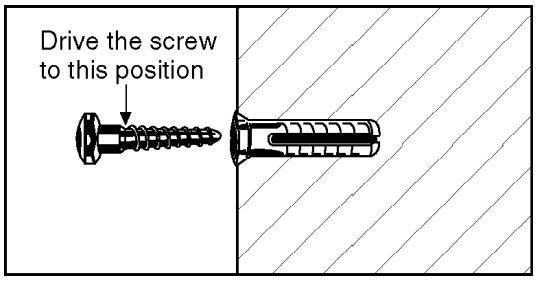
To Mount on Concrete or Mortar Walls:

1. Place the template (included) on the wall to mark the 3 screws positions.

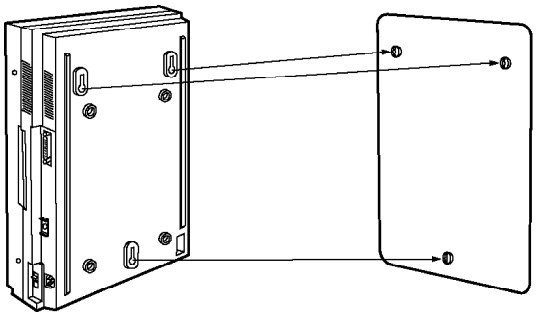
2. Drill 3 holes and drive the anchor plugs (included) with a hammer, flush to the wall.



3. Install the 3 screws into the anchor plugs.



4. Hook the unit on the screw heads.



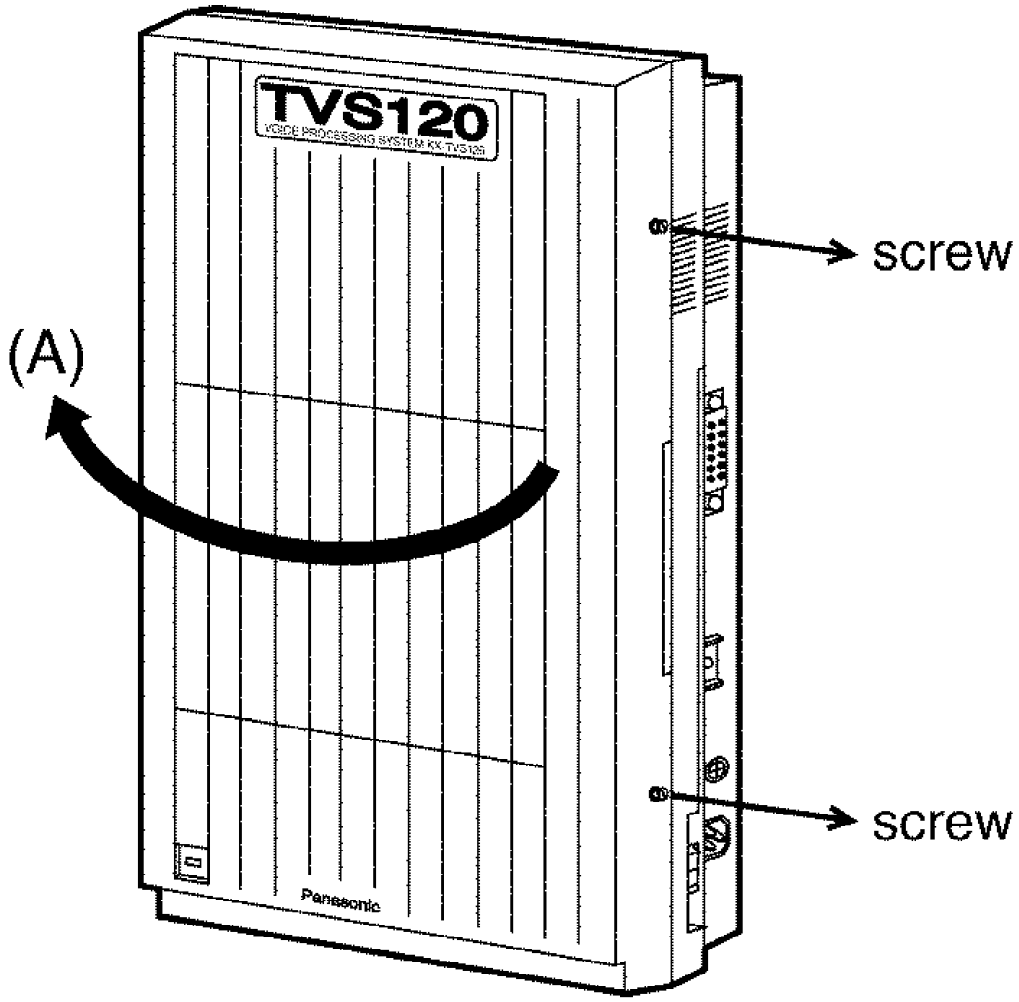
4.3. CONNECTING FROM THE VPS TO THE PBX EXTENSIONS

The VPS must be connected to PBX extension lines. If you have a Panasonic KX-T series PBX and make use of DPT Intregration, use a 4 conductor wiring cord. If you have another type PBX, use a 2 conductor wiring cord. The maximum length of the wire varies according to your PBX type. Please refer to your PBX Installation Manual. Remember the connected extension port number on the PBX. You will call it when accessing one of the assigned incoming call services. The following models are recommended for connecting to the VPS:

- Panasonic KX-T30810, KX-T61610, KX-T123211D, KX-TD816
- Panasonic KX-TD1232, KX-T336100, KX-T96100, KX-TD500
- Panasonic KX-TD308, KX-TA624, KX-TA1232

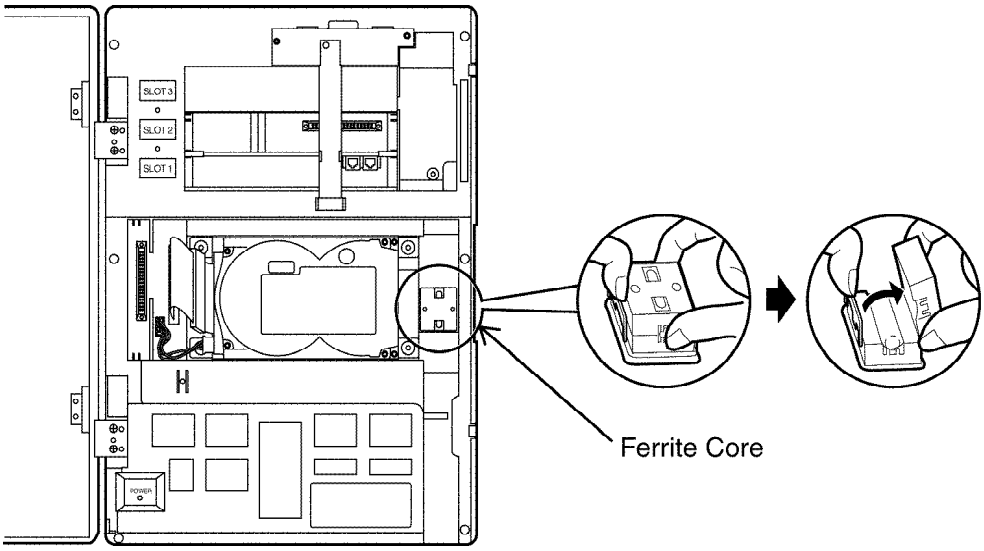
4.3.1. Connecting procedure

Procedure(1)
Loosen two screws on the right side of the main unit, then open the front cover in the direction of arrow (A).



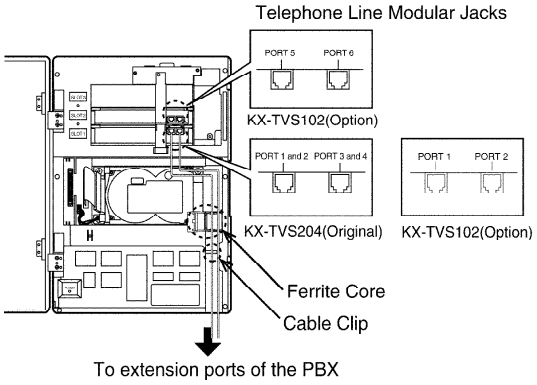
Note:
The screws are attached to the front cover with springs so that they will not be lost.

Procedure(2)
Insert a screwdriver into the opening of the ferrite core and open it.
Lift the right end of the cable clip with your finger as shown below:



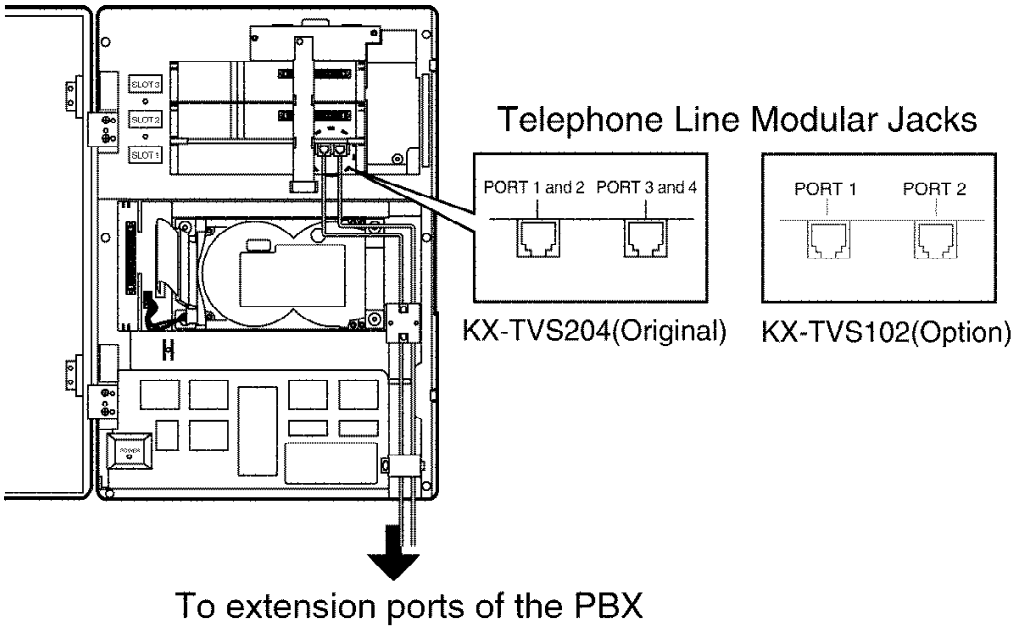
Procedure(3)

Insert the modular plug of the telephone cord into the modular jack on the Port card. Let the telephone cord through the ferrite core and under the cable clip.



Procedure(4)

Then close the ferrite core.



4.3.2. Port of KX-TVS120

You can use the following two kinds of Port cards in the KX-TVS120. The KX-TVS204(DPT Interface Card) is installed in slot1 at the factory.

- 4 Digital ports expansion card (KX-TVS204)

- 2 Digital/Analog ports expansion card (KX-TVS102)

- One KX-TVS204(DPT Interface Card) (2 jacks) can support 4 VPS ports under DPT integration mode only, and KX-TVS204 does not work under Inband/None integration mode.

- One KX-TVS102(DSP/CO Card) (2 jacks) can support 2 VPS ports under any integration mode.

The Number of Ports VPS Cards can support

Card Type	Integration Mode	
	DPT	Inband/None
KX-TVS102	2	2
KX-TVS204	4	Not available

Note:
You can use only one Integration mode among DPT, Inband, and None.
To set the Integration mode, please see Installation Manual.

- For example, when you mount the KX-TVS102 in SLOT1, the VPS

supports only Port1 and Port2. When the VPS administrator sets up parameters for any port [Refer to Installation Manual], please be careful to set up for the proper port number of VPS ports.

DPT Integration
To the Panasonic KX-TD series PBX, the VPS ports look like digital extensions.
The digital communication (2B+D) provides two VPS ports for each Digital Station port of the PBX. For example, when you mount two KX-TVS102, you can use 4 VPS ports in total by connecting 2 jacks of the KX-T series PBX with DPT to 2 jacks of the KX-TVS120.

Note:

1. **To use DPT Integration, the lowest jack of the KX-TVS120 must be connected to the lowest number jack assigned as a Voice Mail Port Assignment in KX-T series. Please see the following connection examples.**
2. **KX-TVS204 is not available to install to the Slot2.**

Card configuration (DPT integration)

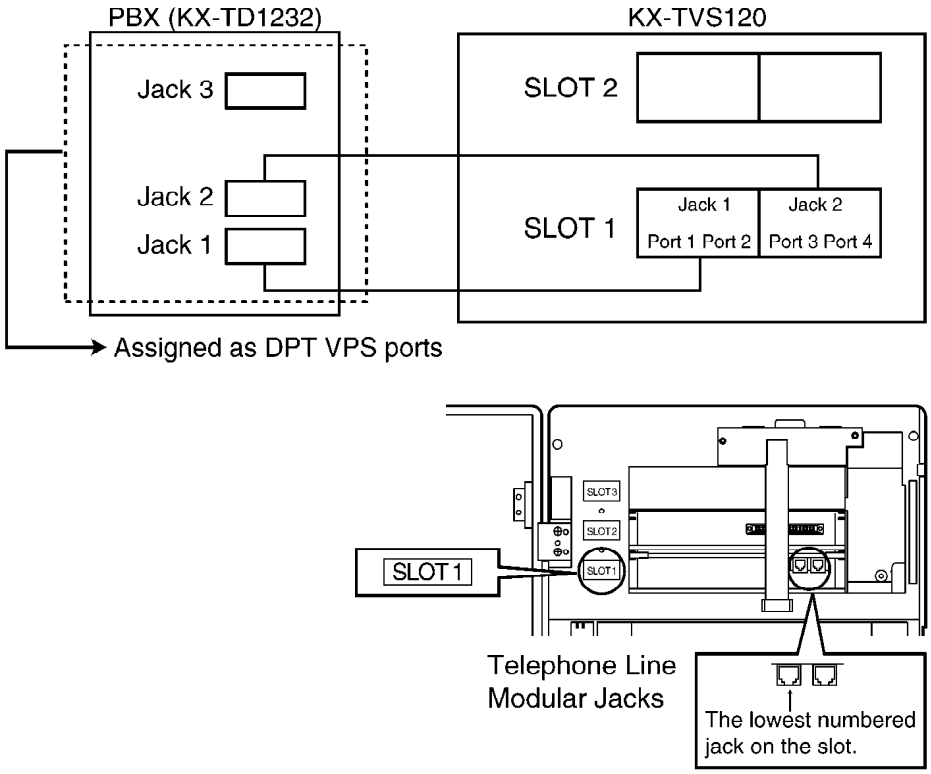
Pattern No.	SLOT1	SLOT2	Total Number of Ports
1	TVS204(Port 1,2,3,4)		4
2	TVS204(Port 1,2,3,4)	TVS102(Port 5,6)	6
3	TVS102(Port 1,2)		2
4	TVS102(Port 1,2)	TVS102(Port 5,6)	4

Card configuration (Inband/None integration)

Pattern No.	SLOT1	SLOT2	Total Number of Ports
1	TVS102(Port 1,2)		2
2	TVS102(Port 1,2)	TVS102(Port 5,6)	4

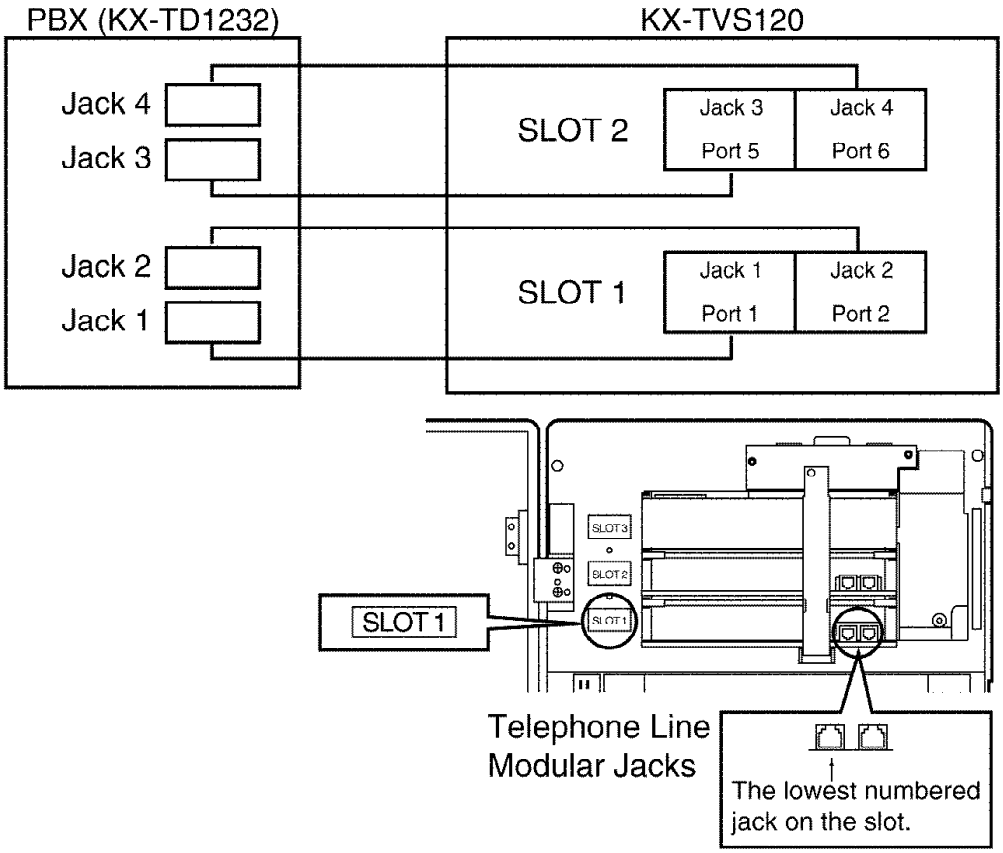
4.3.3. CONNECTION EXAMPLES

(1) Connection Example (SLOT1:KX-TVS204, SLOT2:NO, DPT Integration Mode)



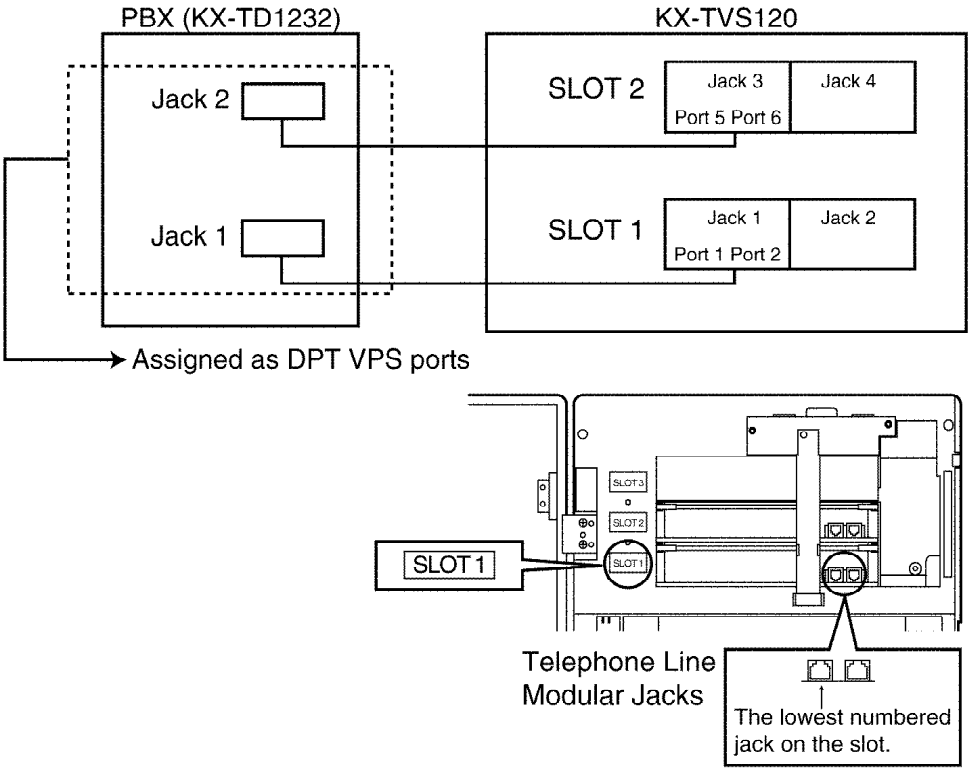
Connect each jack on the KX-TVS204 to your PBX (see the diagram above).
The VPS will support 4 ports for KX-TVS204, with only one jack connected.

(2) Connection Example (SLOT1:KX-TVS204, SLOT2:KX-TVS102 DPT Integration Mode)



Connect each jack on the KX-TVS204 and the lowest-numbered jack on the KX-TVS102 card to your PBX (see the diagram above). The VPS will support 6 ports for KX-TVS204 and KX-TVS102, with 3 jack connected.

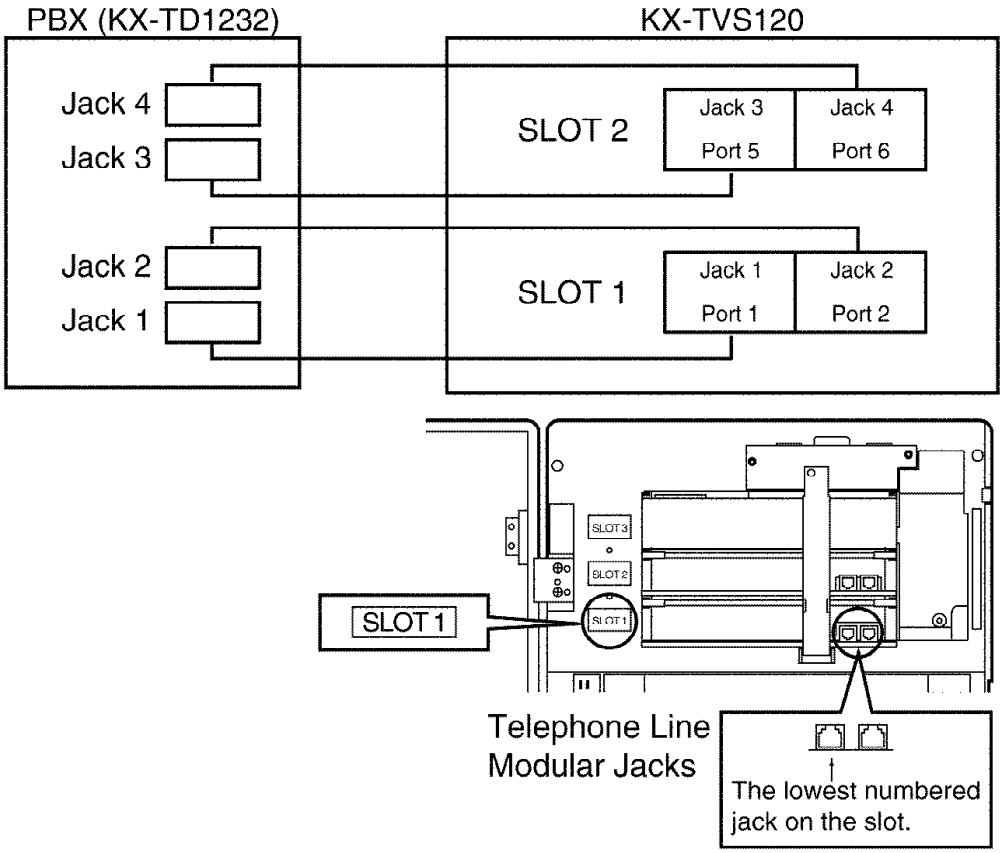
(3) Connection Example (SLOT1:KX-TVS102, SLOT2:KX-TVS102 DPT Integration Mode)



Connect the lowest-numbered jack on the KX-TVS102 to your PBX (see the diagram above). The VPS will support 4 ports for tow KX-TVS102, with 2 jack connected.

Note:
Do not connect the higher-numbered jacks on the KX-TVS102.

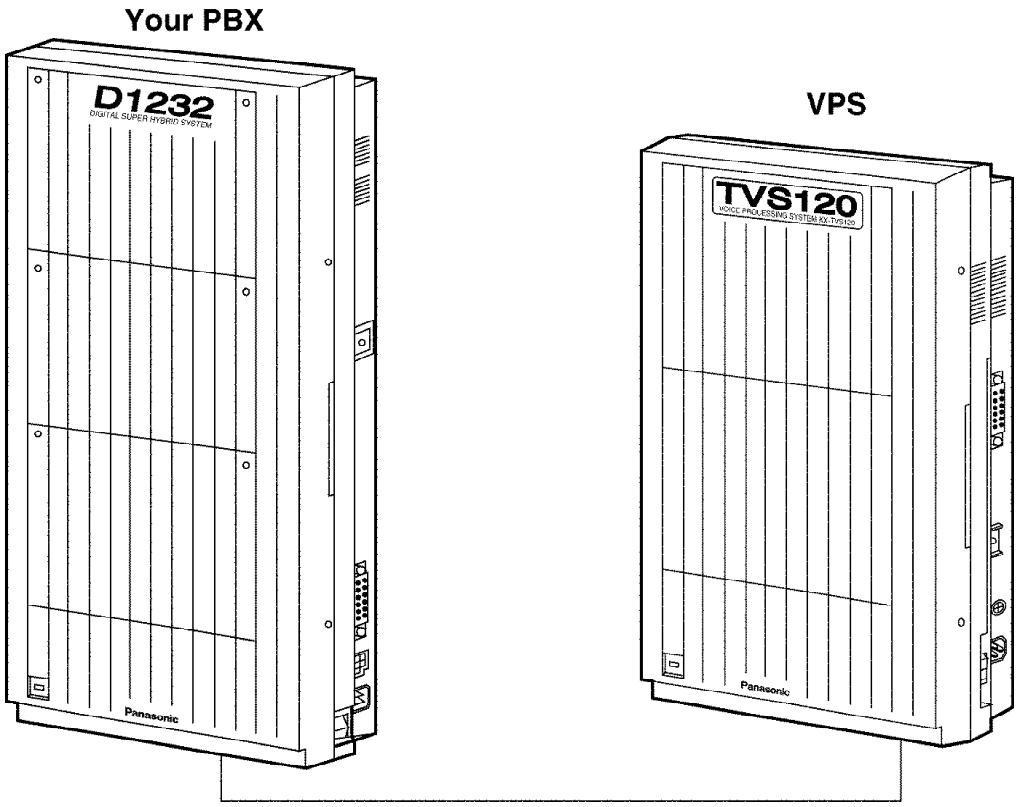
(4) Connection Example (SLOT1:KX-TVS102, SLOT2:KX-TVS102 Inband/None Integration Mode)



Connect both jacks on the KX-TVS102 to your PBX (see the diagram above). The VPS will support 4 ports for two KX-TVS102, with 4 jacks connected.

4.3.3.1. Telephone connections

1. Connect the telephone line to the extension port of the PBX by following instructions below.



2. Close the front cover of the VPS system (and PBX if the cover is removed).
Reverse the procedure of step 1.
3. Tighten the two screw firmly.
Reverse the procedure of step 1.

4.4. CONNECTING A DATA TERMINAL

For the system administration (system set-up, mailbox setup, and system diagnosis), the VT 100 or ASCII terminal must be connected to a serial interface (EIA port) of the VPS. If using DEC VT100 or VT100 compatible terminal, the system administrator program provides the conversational menu-driven environment. If you wish to output reports to a printer, also connect to the VPS and the printer using the EIA port. The wiring and parameters are the same as those for a terminal. The default communication parameters of the VPS are shown as follows.

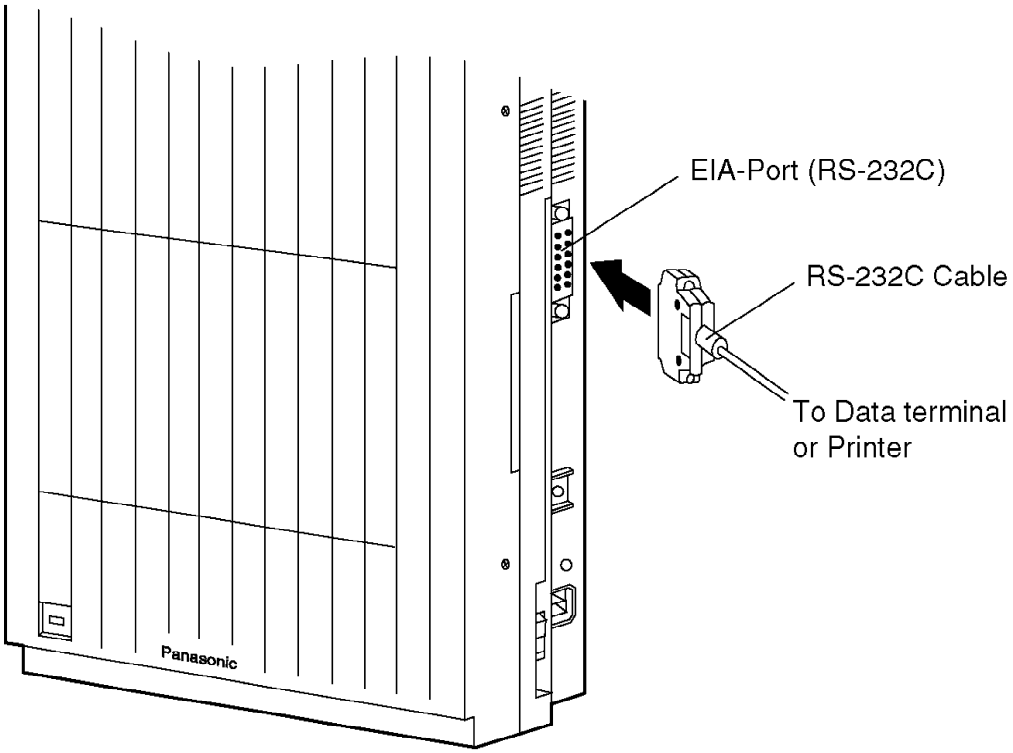
RS-232C parameters

- **Baud Rate: 9600 bps**
- **Word Bit Length: 8 bit**
- **Parity: None**
- **Stop Bit Length: 1 bit**

Connecting RS-232C cable

Precaution

Before connecting the cable, make sure to turn off the power switch on both data terminals and the VPS.



Insert the RS-232C cable into the VPS with the connector indicating the same direction.

Printer Connection

1. Make cables so that the printer may be connected to the VPS as shown in the following chart. Cable must be shielded and the maximum length is 2m (6.5 feet).

Connection Chart:

EIA (RS-232C) port on the VPS				EIA (RS-232C) port on the Printer		
Circuit Type (EIA)	Signal Name	Pin No.		Pin No.	Signal Name	Circuit Type (EIA)
AA	FG	1	←	1	FG	AA
BA	TXD	2	→	3	RXD	BB
BB	RXD	3	←	2	TXD	BA
AB	SG	7	←	20	DTR	CD
CD	DTR	20	→	7	SG	AB
			→	5	CTS	CB
			→	6	DSR	CC
			→	8	DCD	CF

The pin configuration of the EIA (RS-232C) connector is as follows.

Pin No.	Signal Name		Circuit Type	
			EIA	CCITT
1	FG	Frame Ground	AA	101
2	TXD	Transmitted Data	BA	103
3	RXD	Received Data	BB	104
4	RTS	Sound	CA	105
6	DSR	Ready	CC	107
7	SG	Signal Ground Data	AB	102
8	DCD	Carrier Defect	CF	109
20	DTR	Data Terminal Ready	CD	108.2

(Reference)
EIA (RS-232C)
SIGNALS

Frame Ground (FG)
Connects to the unit frame and the earth ground conductor of the AC power cord.

Transmitted Data (TXD) .....(output)
Conveys signals from the unit to the printer (or terminal). A "Mark" condition is held unless data or BREAK signals are being transmitted.

Received Data (RXD)..... (input)
Conveys signals from the printer (or terminal).

Request To Send (RTS) .....(output)
This lead is held on whenever DSR is on.

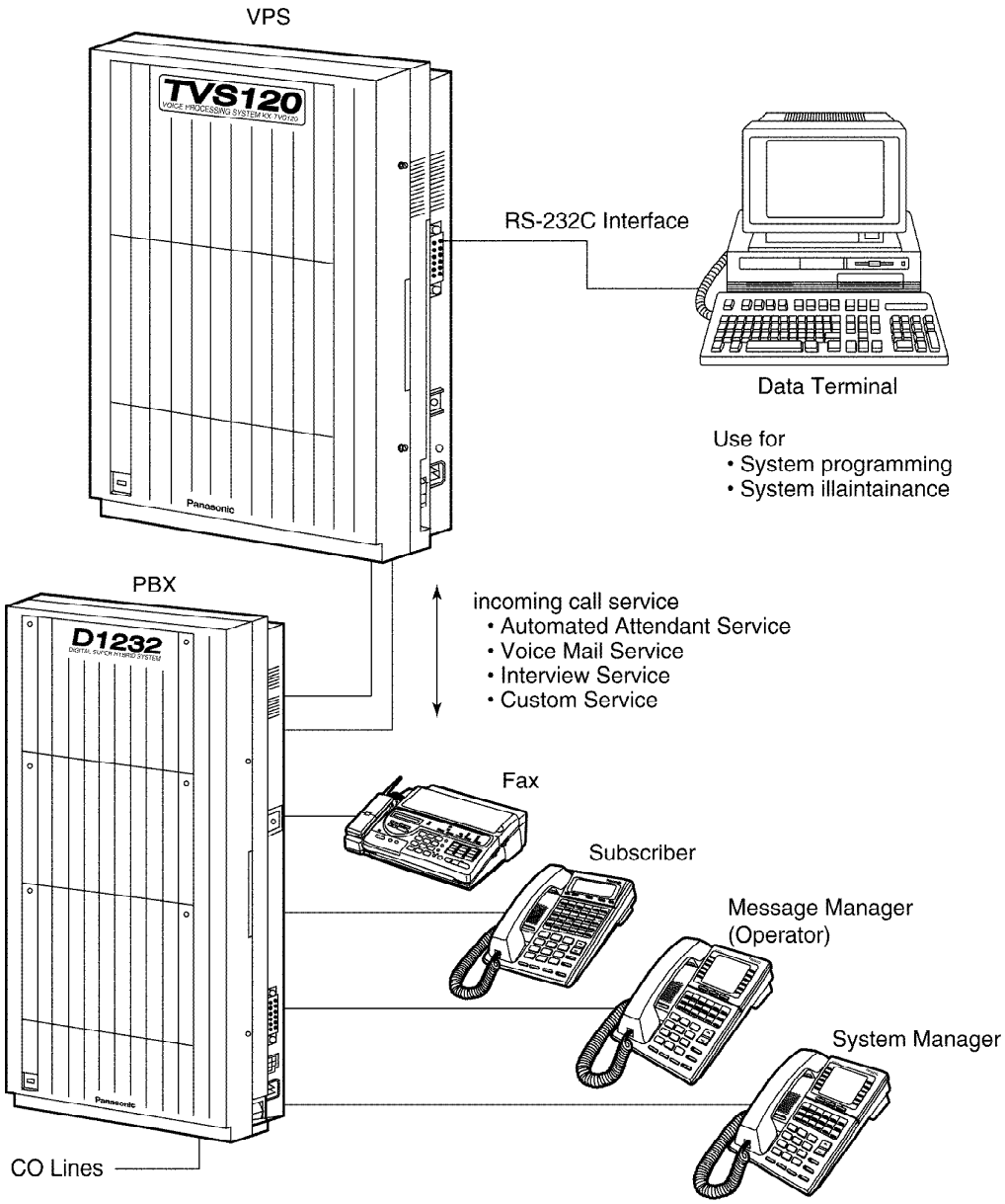
Signal Ground (SG)
Connects to the DC ground of the unit for all interface signals.

Data Terminal Ready (DTR)..... (output)
This signal line is turned ON by the unit to indicate that it is ON LINE. Circuit DTR ON does not indicate that communication has been established with the printer (or terminal). It is switched OFF when the unit is OFF LINE.

4.5. POWER CABLE CONNECTION

Attach the AC jack at the cord to AC inlet of the VPS.
Before connecting the power cable to an AC outlet, make sure all other connections (RS-232C data terminal with VPS, PBX with VPS, PBX with telephone lines) are secure, and front cover is closed firmly. Use the AC outlet dedicated to the VPS unit.

Example:



4.6. SYSTEM PROGRAMMING

For the details of the system programming, refer to "Installation Manual".

4.7. STARTING THE SYSTEM

Turn on the power switch, the VPS will start up in the following sequence.

Display of usual start-up

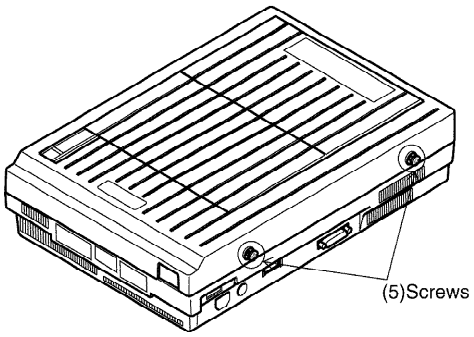
```
CARD TEST ...
SYSTEM SETUP ...
    1. .      2. .

    Active COs       :   1   2   3   4
   DPT Interface Connection is Established
  ** ON LINE MODE **
>
```

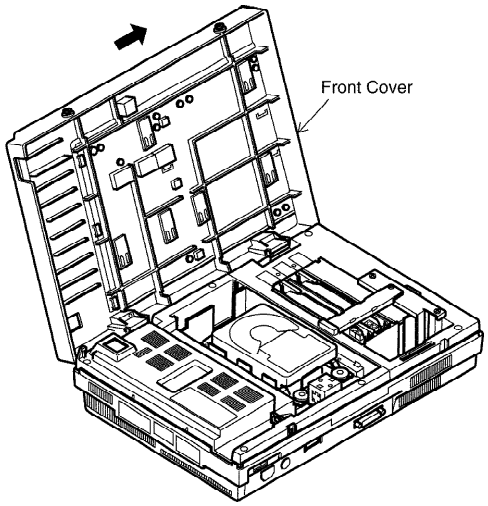
5. DISASSEMBLY INSTRUCTIONS

5.1. HOW TO REMOVE THE FRONT COVER

Procedure 5.1.

1. **Loosen the two Screws (5).**
2. **Open the Front Cover.**
3. **Slide the Front Cover in the direction of the arrow when removing it.**

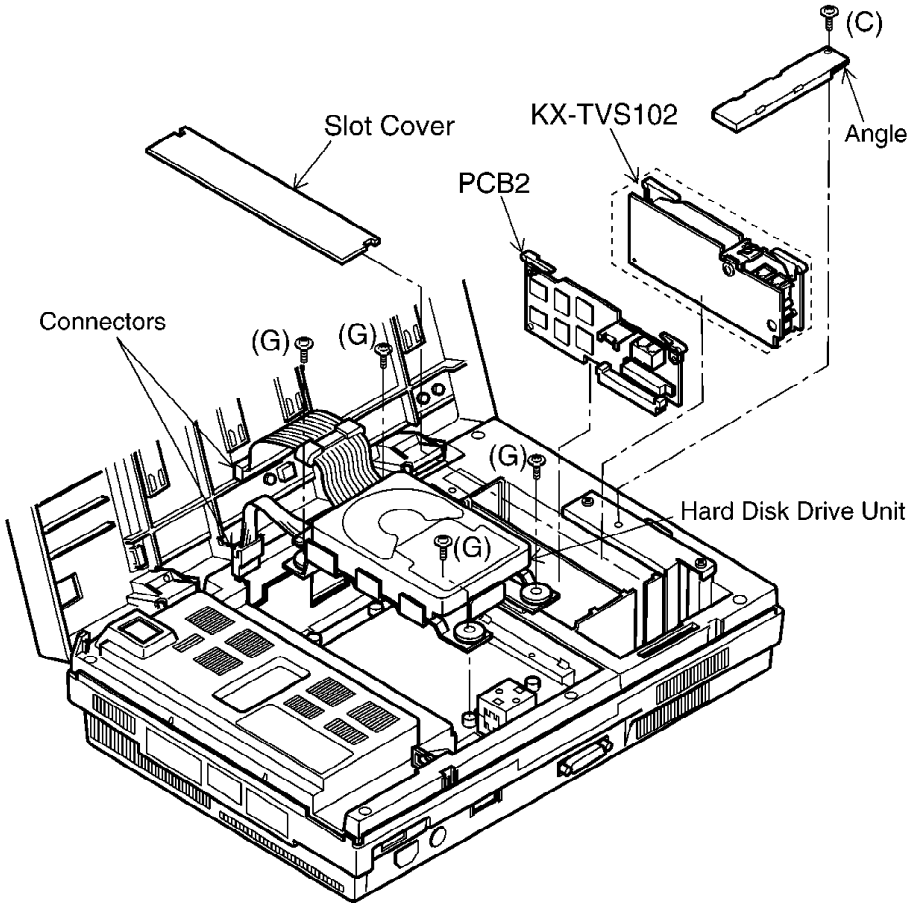




5.2. HOW TO REMOVE THE HARD DISK DRIVE UNIT, PCB2(KX-TVS204)(DPT INTERFACE CARD) AND OPTION(KX-TVS102)(DSP/CO CARD)

Procedure 5.1. → 5.2.

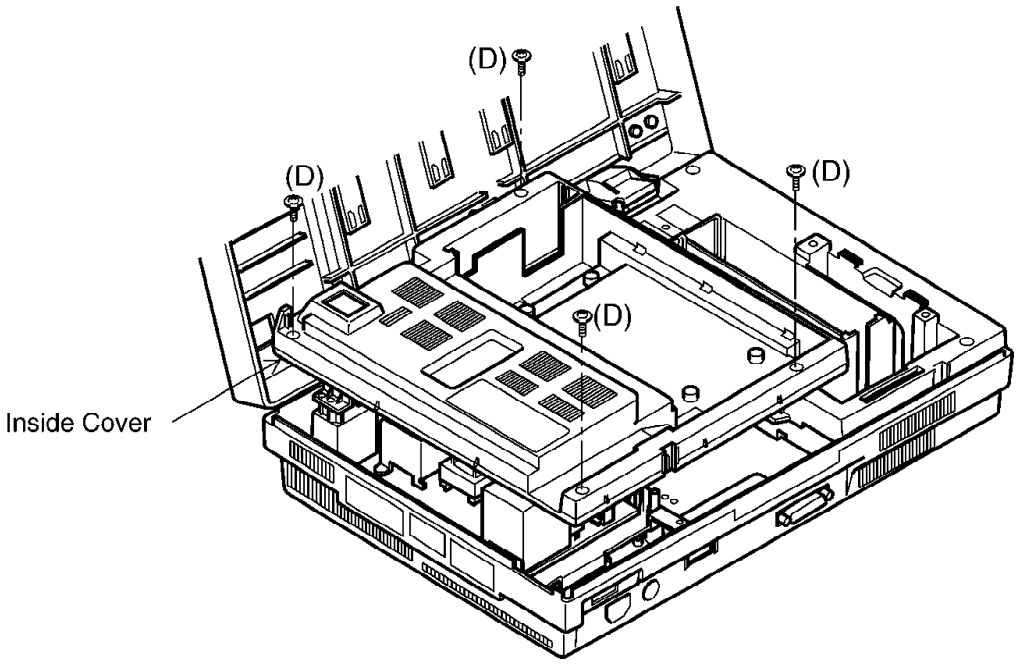
1. Remove the four Screws (G).
2. Pull out the two Connectors.
3. Remove the Hard Disk Drive Unit.
4. Remove the Screw (C).
5. Remove the Angle.
6. Remove the PCB2(KX-TVS204)(DPT Interface Card) and Option(KX-TVS102)(DSP/CO Card).



5.3. HOW TO REMOVE THE INSIDE COVER

Procedure 5.1. → 5.2. → 5.3.

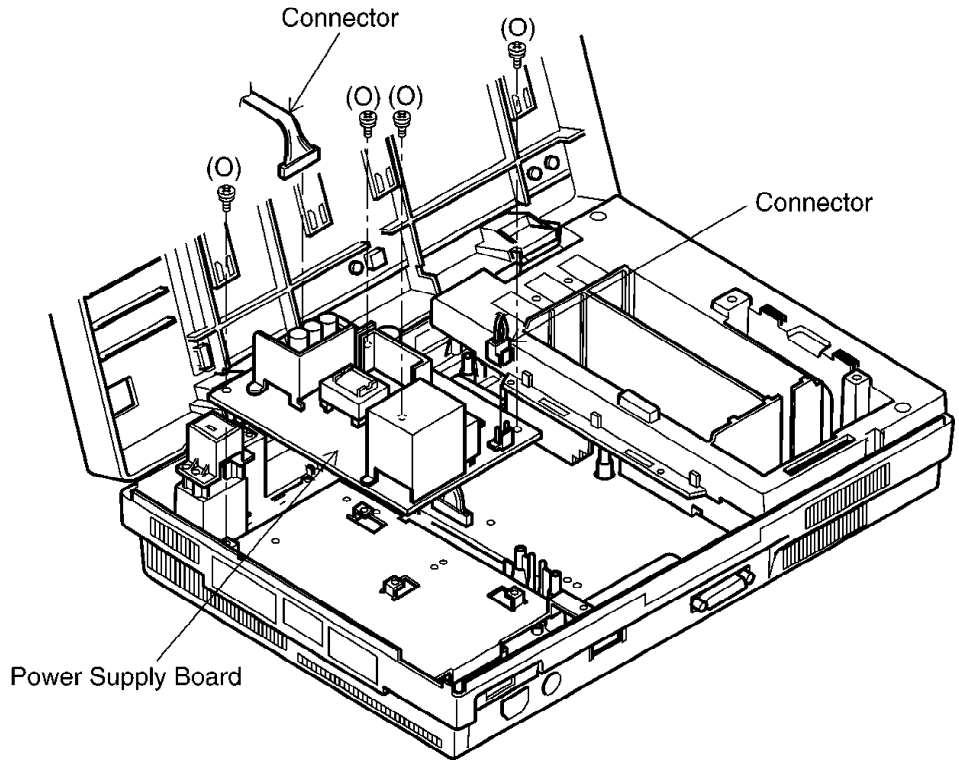
1. Remove the four Screws (D).
2. Remove the Inside Cover.



5.4. HOW TO REMOVE THE POWER SUPPLY BOARD

Procedure 5.1. → 5.2. → 5.3. → 5.4.

1. Remove the four Screws (O).
2. Remove the two Connectors.
3. Remove the Power Supply Board.

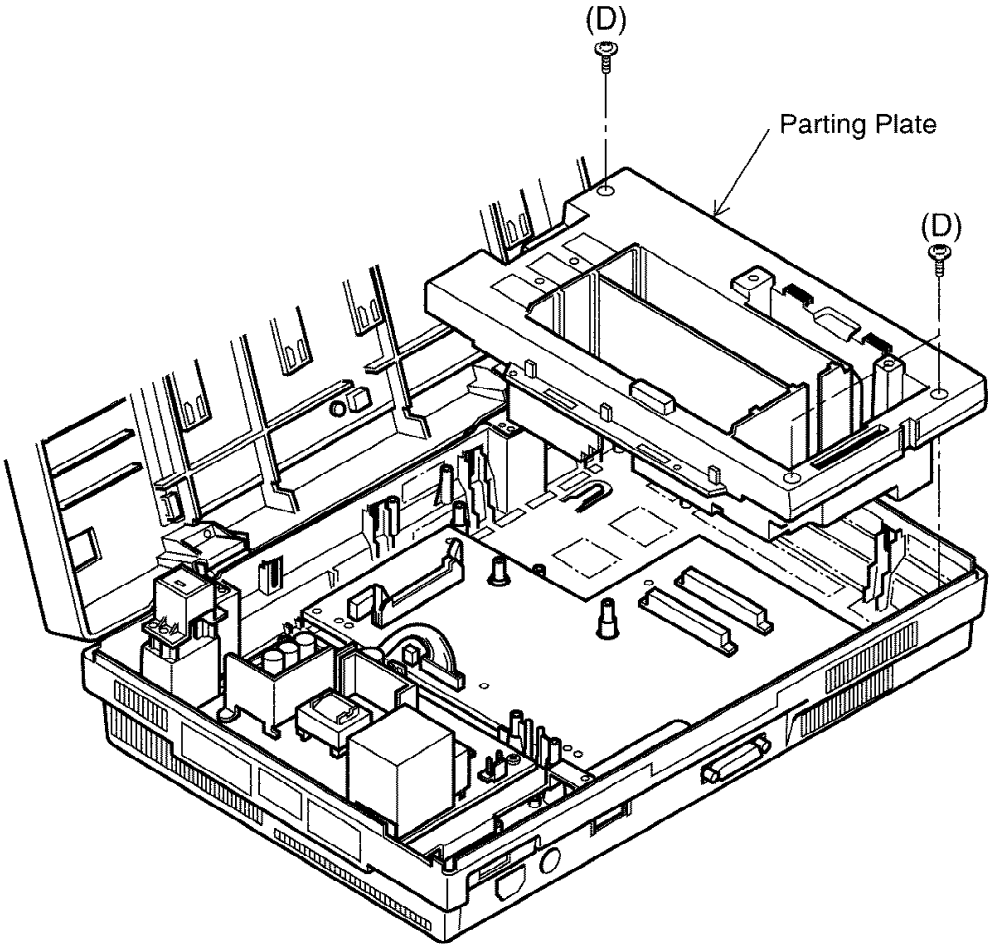


5.5. HOW TO REMOVE THE PARTING PLATE

Procedure 5.1. → 5.2. → 5.3. → 5.5.

1. Remove the three Screws (D).

2. Remove the Parting Plate.



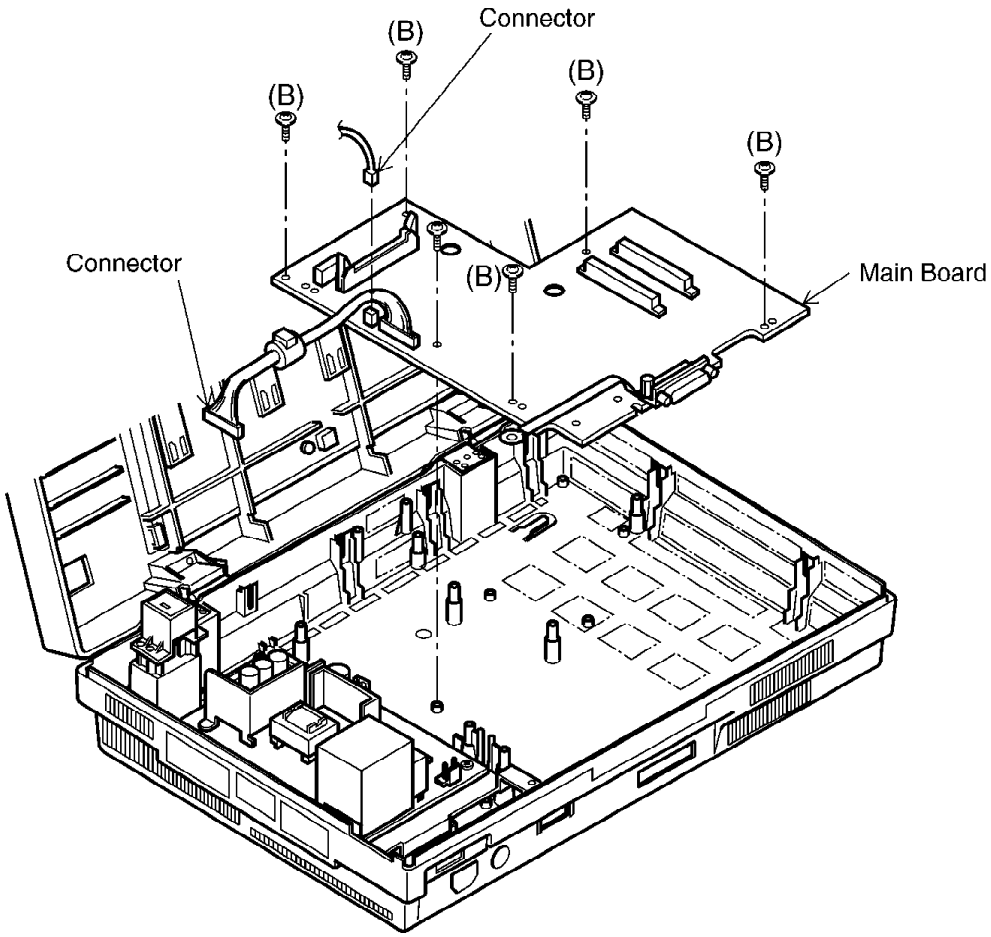
5.6. HOW TO REMOVE THE MAIN BOARD

Procedure 5.1. → 5.2. → 5.3. → 5.5. → 5.6.

1. Remove the six Screws (B).

2. Pull out the two Connectors.

3. Remove the Main Board.



6. HOW TO REPLACE THE FLAT PACKAGE IC

If you do not have the special tools (for example: SPOT HEATER) to remove the SPOT HEATER'S Flat IC, if you have solder (large amount) a soldering iron and a cutter knife, you can easily remove IC's even though large than 100 pin.

6.1. PREPARATION

- SOLDER

Sparkle Solder 115A-1, 115B-1 or Almit Solder KR-19, KR-19RMA

- Soldering iron

Recommended power consumption is between 30 W to 40 W.
Temperature of Copper Rod 662 ± 50°F (350 ± 10°C)
(An expert may handle a 60~80 W iron, but beginner might damage foil by overheating.)

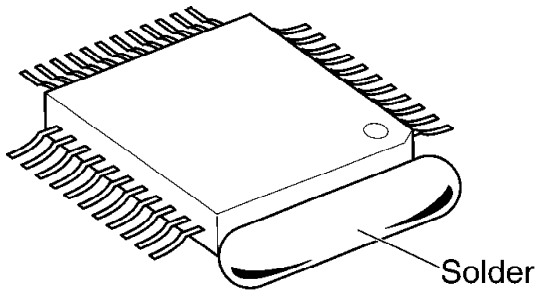
- Flux

HI115 Specific gravity 0.863
(Original flux should be replaced daily.)

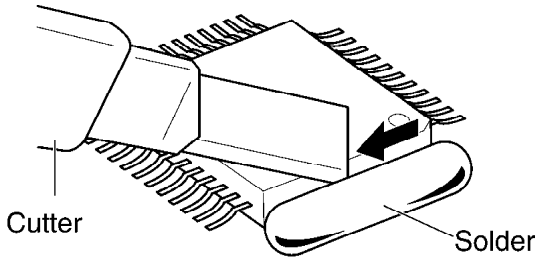
6.2. FLAT PACKAGE IC REMOVE PROCEDURE

1. When all of the IC lead can not been seen at the standard degree, fill with large quantities of solder.

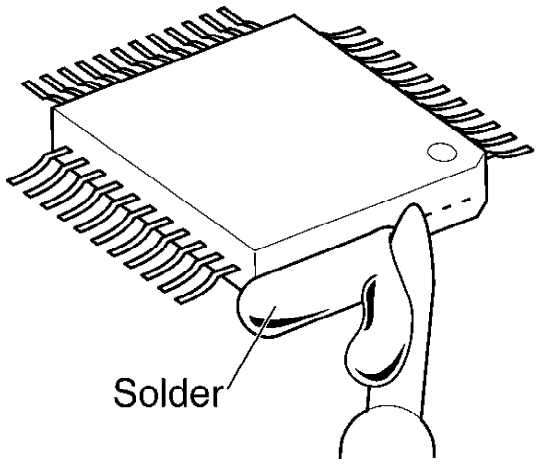
Note:
If you do not fill with solder and directly cut the IC lead with the cutter, stress may build up directly in the P.C.board's pattern. If you do not fill with large quantities of solder as in step 1 the P.C.board pattern may be removed.



2. Using a cutter, cut the lead at the source. (Cut the contents with the cutter lightly 5 or 6 times.)



3. Remove when the solder melts. (Remove the lead at the same time.)

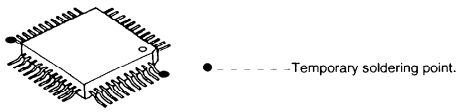


After removing the Flat IC and when attaching the new IC, remove any of the excess solder on the land using the soldering wire, etc. If the excess solder is not removed from the land, the IC

will slip and not be attached properly.

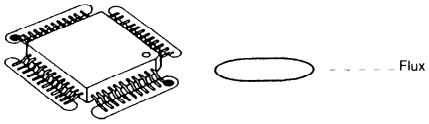
6.3. FLAT PACKAGE IC INSTALLATION PROCEDURE

1. Temporary fix FLAT PACKAGE IC by soldering on two marked pins.

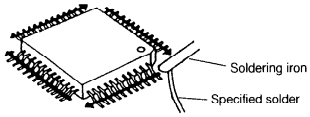


***Check the accuracy of the IC setting with the corresponding soldering foil.**

2. Apply flux for all pins of FLAT PACKAGE IC.



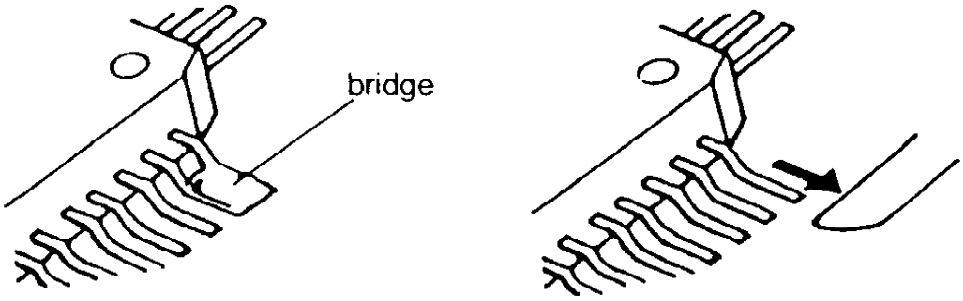
3. Solder using the specified solder, in the direction of the arrow, by sliding the soldering iron.



6.4. BRIDGE MODIFICATION PROCEDURE

1. Lightly re-solder the bridged portion.

2. Remove the remaining solder along pins using a soldering iron as shown in the figure below.



7. FUNCTIONAL BLOCK DIAGRAM

(SLOT1: KX-TVS204)

(SLOT1: KX-TVS204, SLOT2:KX-TVS102)

(SLOT1: KX-TVS102, SLOT2: KX-TVS102)

7.1. SYSTEM SPECIFICATIONS

SYSTEM SPECIFICATIONS

ITEM	DESCRIPTIONS	
Cabinet	Wall mounted type stand-alone style	
Dimension (H × W × D)	470 × 335 × 110 mm (18-1/2" × 13-3/16" × 4-21/64")	
Weight	Approximately 5.2 kg (11.46lb) (with 1 KX-TVS204 card installed at the factory	
Power Source	AC 120 V, 60 Hz	
Voice Storage Capacity	32 hours	
Line Capacity Line connector Line interface (Option)	KX-TVS204(DPT Interface Card)(Original) 4 ports 4 pin modular jack type connector Port-A: CH1,CH2 DPT interface Port-B: CH2,CH4 DPT interface	KX-TVS102(DSP/CO Card)(Option) 2 ports 4 pin modular jack type connector Port-A: DPT/SLT Hybrid interface Port-B: SLT interface
Data Terminal Interface	RS-232C Port (25 pin Dsub connector) × 1 Baud Rate: 300 up to 38,400bps (programmable)	
Operation Switches	Power Switch × 1	
	Rotary Switch (Mode Configuration Switch) × 1 (only maintenance use)	
LED	Power Indicator (red) × 1	
Dialing Method	Tone duration/Pulse (10/20 pps) *	
Flash time	100/300/600/900 msec (programmable) *	
CPC detection	None/6.5/150/300/450/600 msec (programmable) *	
Extension numbering	2 to 5 digits (programmable)	
Pause time	1 to 9 s (programmable)	
Message Waiting Lamp	Programmable DTMF sequence, or DPT data line	
Number of Mailboxes	maximum 64	
Number of Messages	100 per mailbox (programmable)	

Personal Greeting Message Length	**8 to 60 s (programmable)**
Message Retention Time	**New message : 1 to 30 days**
	Old message : 1 to 30 days or unlimited
Message Length	**1 to 6 min. or unlimited (programmable)**
Reports output	**Mailbox list, Class of Service list, System Service report, Call Account report, Port Usage report, Mailbox Usage report, FAX report**

*** Using with SLT interface (KX-TVS102)**

7.2. MAIN BOARD

The Main Board serves as the main controller of the KX-TVS120, and it incorporates a CPU (TMP68301/16 MHz: IC301) which is 68HC000-compatible. This CPU comes with a built-in serial port (RS-232C), parallel port, timer and interrupt controller.
Installed as the base memory are an 8M-bit flash ROM (IC308) and a 2MB RAM (IC304/305/307/309). The system initialize program, self-diagnosis execution program and the program for booting the system from the hard drive are stored in the ROM. The RAM is used for system program execution and voice buffer purposes.
A calendar IC (IC308) which is backed up by a battery is mounted on this card to provide time information.
The following external interfaces are provided: an IDE type hard disk interface (1 slot) enabling up to 2 units to be controlled, an asynchronous communication RS-232C interface (1 port) supporting transfer rates up to 38.4 kbps, an I/O card expansion bus (2 slots: CN302/303) for connecting existing line interface module KX-TVS102 and 4port DPT interface cards KX-TVS204. The expansion bus for connecting the line interface consists of an 8-bit slave I/O bus and a DMA data transferable serial voice channel bus. The serial voice channel bus is an original bus which is capable of transferring 3 kinds of serial data for 32 channels. The transfer data includes PCM data (max. 64 kbps: DPD and UPD signals), voice data (max. 32 kbps: UVD and DVD signals), and PT data (max. 32 kbps: UVA, UVC and DVC signals). The PCM data is connected to the remote modem interface, and after it has been restored to analog signals on the remote modem card, it is supplied to the modem IC to enable modem transmission. DMA transfer of the voice data with the main memory is enabled by combining it with the DMA channel.
The KX-TVS120 accommodates two KX-TVS102, or one KX-TV204 in slot1 and one KX-TVS102 in slot2 modules which can be installed in its expansion slots. Its port expendability extends up to maximum 6 ports with DPT interface.

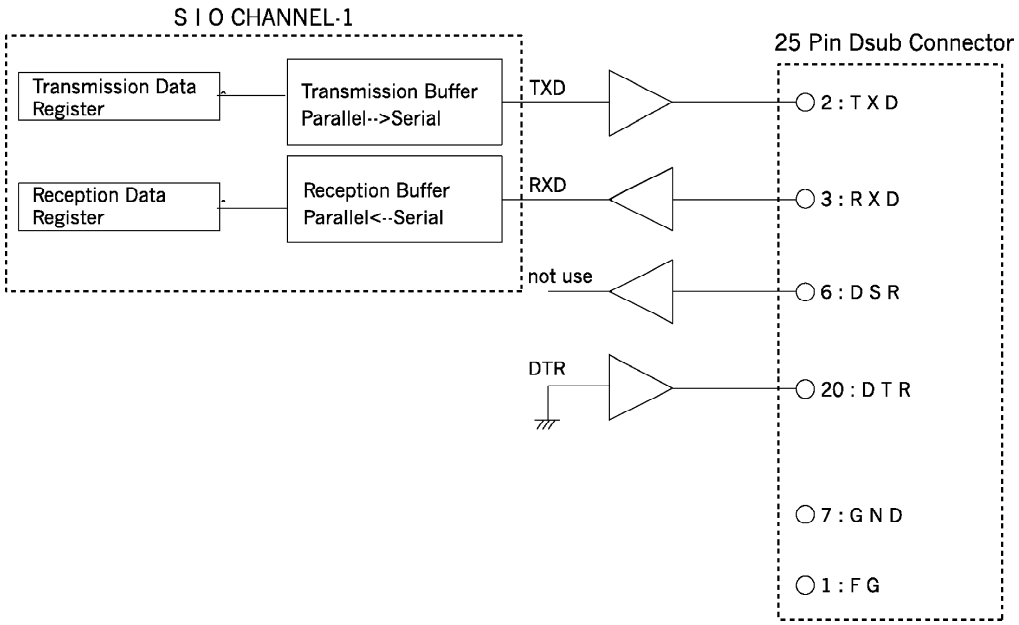
SPECIFICATIONS OF THE MAIN BOARD

BLOCK	SPECIFICATIONS	DESCRIPTIONS
CPU	68EC000 compatible	Running frequency : 16.384 MHz (IC301)
RAM (DRAM)	2.0M byte	4Mbit Dynamic RAM × 4 (IC304/IC305/IC307/ IC309)
ROM	512k byte	4Mbit Flash ROM ×1 (IC306)
RAM (SRAM)	1.0M byte	4Mbit S-RAM ×2 (IC331/IC332)
INTERRUPT CONTROLLER	7 levels	hardware interrupt request notify to CPU (IC301)
TIMER	3 Channels	for using the system management (IC301)
RS-232C I/F	1 Channels	Asynchronous (300 - 38.4kBPS) (IC301)
Parallel I/O Port	13 bit	for using LED on/off, Rotary Switch sensing (IC301)
DPT I/F	CCITT X.25 Level-2	DPT Protocol Control (IC303)
System Controller	Custom LSI	for the all of the system timing control (IC302)
CLOCK	Real Time Clock	with Battery Backup (IC308)
HDD I/F	40pin connector × 1 (data) 4pin connector × 1 (power)	connecting up to 2 Hard Disk Drives (IC301)
EXP. SLOT	50pin connector × 2	connecting DSP/CO module (CN302 to CN303)

7.2.1. RS-232C INTERFACE

The MC68301 has a separate 3-channel serial interface which supports full duplex asynchronous communication (UART). In the KX-TVS120, channel 0 is used as the remote modem interface and channel 1 as the existing RS-232C interface. Since channel 2 is not used, it is initialized only.
In terms of channel 0, modem control logic has been loaded, and CTS (clear to send), DSR (data set ready), DTR (data terminal ready) and RTS (request to send) control is added. For further details on the remote modem interface using this channel, refer to the next section.
Channel 1 is used as the existing RS-232C interface and controlled only by the TXD and RXD data send/receive signals. It is connected to the 25-pin D-sub connector as indicated below.

RS-232C INTERFACE DIAGRAM



7.3. KX-TVS102 (DSP/CO CARD)

7.3.1. DSP CARD (KX-TVS102)

DSP block is loaded with DSP (IC109) installed with a 1.3k word RAM and 32k word outside the fixed program ROM (IC107/IC108).
This DSP interfaces CODEC, connected with a SLT interface on a CO block and transforms voice region signals D/A, A/D, and DPT line.
Each DSP disposes a digital voice region data for each channel described below. Mutual transformation, voice region digital data (64kBPS : 8bit/125us) and ADPCM data (32kBPS : 4 bit/ 125us), are executed. To detect a certain tone (for example DTMF tone or call progress tone) by analyzing input PCM data and to output a certain tone (for example DTMF tone or BEEP tone) as PCM data.
Timing Control on the DSP block is controlled by the system controller (IC101). System controller includes DPT interface, ADPCM compressed voice data transfer control between DSP and system memory, FIFO logic and parallel I/O port to control the SLT circuit line.
DSP receives commands from the host CPU through FIFO (IC101), then works based on the command.
This DSP execution program is stored in the external high speed ROM (IC107/IC108).
The DPT interface logic works to input and output the information data (D channel data) received and sent with the PBX through DPT with a HDLC controller (IC303) on a CPU block. It distributes voice region data (B1,B2 channel data) received and sent by the PBX through a DPT to each DSP(IC109A, IC109B).
The Parallel I/O port, used for SLT interface on the CO block taking status and Hook control, is controlled by the CPU.

SPECIFICATION OF THE DSP CARD

BLOCK	SPECIFICATIONS	DESCRIPTIONS
HOST I/F	50-pin Connector	Signals × 38, +5V × 2, -5V × 2, GND × 8
CO I/F	30-pin Connector	
DSP LSI (IC109)	PQVIMP58C002	Running frequency : 57.344MHz (14.336MIPS)
	Internal RAM	1312 word × 16 (for Program/Data memory)
	Internal ROM	20kword × 16 (not used)
	Serial Port	using DPT digital voice data in/out
	CODEC I/F	using SLT analog voice data in/out
DSP ROM (IC107/IC108)	64kByte (IC107/IC108)	access time : 35nsec
SLAVE CONTROLLER (IC101)	FIFO	To communicate between Host CPU and DSP
	Parallel I/O Port	bit IA-3 : not used IA-2 : CPU-A detect when 0 IA-1 : not used IA-0 : BELL-A detect when 0
		OA-1 : not used OA-0 : HOOK-A control (0: off-hook)
		IB-3 : not used IB-2 : CPU-B detect when 0 IB-1 : not used IB-0 : BELL-B detect when 0
		OB-1 : not used OB-0 : HOOK-B control (0: off-hook)
		OX-3 : not used OX-2 : not used OX-1 : loop test enable when 0 OX-0 : not used
	Serial Voice Port	for ADPCM Voice Data Transfer Control between DSP ar System Memory
	DPT interface	DPT Frame Formatter and Transceiver

7.3.2. CO CARD (KX-TVS102)

A port in the CO block is a hybrid component and is constructed to add an SLT interface with loop start style to the DPT transceiver.
It is intended to detect the arrival of signals (BELL), to catch circuits (DC loop enable), and to generate a dial pulse by loop on/off and 2-line ~ 4-line transformation (Balance-Network) as a basic function. The 4-line analog data is transformed to digital data by CODEC, then is interfaced with the DSP block.
The DPT transceiver includes the transceiver by transistor (Q261/Q262) and receiver by converter (IC261) and interfaces with PBX through the Pulse Trans (T291).

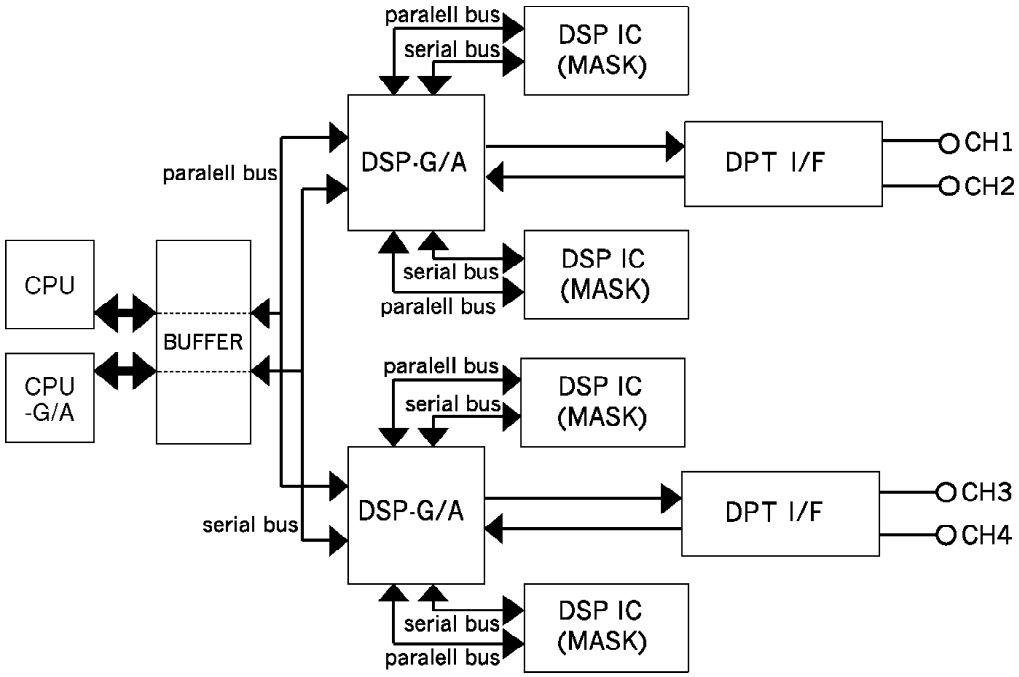
SPECIFICATIONS OF THE CO CARD

<table>
<tr><th>BLOCK</th><th>SPECIFICATIONS</th><th>DESCRIPTIONS</th></tr>
<tr><td>DSP I/F</td><td>30-pin Connector</td><td></td></tr>
<tr><td>CO I/F</td><td>4 pin Modular × 2</td><td>Port-A : DPT/SLT Hybrid I/F
Port-B : SLT I/F</td></tr>
<tr><td>T-R I/F</td><td>BELL Detect</td><td>To Detect the following Bell Signal
Voltage : min. 40 Vrms (Frequency : 25 Hz)
The H/W only detects the level/frequency.
The bell cadence should be checked by software algorithm.</td></tr>
<tr><td></td><td>DIAL PULSE Control</td><td>The hardware logic only controls the loop ON/OFF.
Pulse Dialing Cadence is controlled by S/W
Dialing Rate : 10 or 20 PPS
Break to Make Ratio : 60 %
Interdigit Interval : Typical 800 ms</td></tr>
<tr><td></td><td>DTMF TONE Dialing</td><td>DTMF tone is generated by DSP LSI, and DSP sends the DTMF tone to CODEC or D-PITS.
-Tone Level : High Group : -9 dbm
Low Group : -11 dbm
Twist 2 dbm
Harmonics Level: -7 dbm
-Digit Layout : Refer to following Table
High Group [Hz]
<table><tr><th></th><th></th><th>1209</th><th>1336</th><th>1477</th><th>1633</th></tr><tr><td>Low Group</td><td>697</td><td>1</td><td>2</td><td>3</td><td>A</td></tr><tr><td>[Hz]</td><td>770</td><td>4</td><td>5</td><td>6</td><td>B</td></tr><tr><td></td><td>852</td><td>7</td><td>8</td><td>9</td><td>C</td></tr><tr><td></td><td>941</td><td>*</td><td>0</td><td>#</td><td>D</td></tr></table>
-Frequency Tolerance : max +/- 1.5%
-Duration : 80 msec
-Interdigit Interval : 100 msec</td></tr>
</table>

7.4. KX-TVS204 (DPT Interface Card)

DSP block is loaded with masked DSP (IC109) installed with a 1.3k word RAM.
This DSP interfaces and DPT line.
Each DSP disposes a digital voice region data for each channel described below. Mutual transformation, voice region digital data (64kbps : 8bit/125 μ s) and ADPCM data (32kbps : 4 bit/ 125 μ s), are executed. To detect a certain tone (for example DTMF tone or call progress tone) by analyzing input PCM data and to output a certain tone (for example DTMF tone or BEEP tone) as PCM data.
Timing Control on the DSP block is controlled by the system controller (IC101). System controller includes DPT interface, ADPCM compressed voice data transfer control between DSP and system memory, FIFO logic.

DSP receives commands from the host CPU through FIFO (IC101), then works based on the command.
This DSP execution program is stored in the internal ROM.
The DPT interface logic works to input and output the information data (D channel data) received and sent with the PBX through DPT with a HDLC controller (IC303) on a CPU block. It distributes voice region data (B1,B2 channel data) received and sent by the PBX through a DPT to each DSP(IC109A, IC109B).
The Parallel I/O port is controlled by the CPU.
The DPT transceiver includes the transceiver by transistor (Q261/Q262) and receiver by converter (IC261) and interfaces with PBX through the Pulse Trans (T291).
The 4 DPT card with 4 ports is optionally mounted on the KX-TVS120 for DPT interfacing only. It shares the circuit board outline with the existing DSP card of the KX-TVS102(DSP/CO Card). This enables the KX-TVS120 to share its slot cabinet with the KX-TVS102(DSP/CO Card). Along with the single circuit board design, DSP IC masking and the creation of six circuit board layers have been implemented. The general configuration is shown in the illustration below.



The KX-TVS204(DPT Interface Card) has a construction in which the existing KX-TVS102(DSP/CO Card) DPT interface sections are connected through a dual buffer system. Two DSP gate arrays and four mask DSP ICs are mounted as a result. Two ports are provided, and by using only high/low lines, DPT communication for two channels is enabled using a single port, and communication for 4 channels is enabled using two ports.
The host CPU must identify the previously mentioned slot addresses and card identification addresses for the KX-TVS204(DPT Interface Card).

SPECIFICATIONS OF THE KX-TVS204(DPT Interface Card)

BLOCK	SPECIFICATIONS	NOTE
HOST I/F Connector	50pin Connector	Signals × 38, -5V × 2,+5V × 2,GND
DPIT I/F	4pin Modular	Port A : A ch,B ch DPT I/F Port B : C ch,D ch DPT I/F
DSP X 4	PSVI8C060BPJ Internal RAM Internal ROM Serial I/O Parallel I/O SD-CODEC Port 3 channels ADC	Running Frequency : 57.344MHz (14.336MIPS) 1312word × 16 (for program / Data memory) 20kword × 16 (only program memory) DPT PCM voice data in/out B port : not use D port : Transfers data not use not use
DSP ext ROM	32Kword × 16bit	not use by using masked DSP IC
DATA FIFO	4byte/channel	To communicate between Host CPU and DSP
parallel I/O	Total 20bit IA/IB : Readable both DSP & Host OA/OB : Writable only HOST IX/OX : Accessible only HOST	bit IA-3: Card Identity (always 1) bit IA-2: not use (detect 1) bit IA-1: not use (always 1) bit IA-0: not use (detect 1) bit OA-1: not use bit OA-0: not use bit IB-3: Card Identity (always 1) bit IB-2: not use (detect 1) bit IB-1: not use (always 1) bit IB-0: not use (detect 1) bit OB-1: not use bit OB-0: not use bit IX-3: Card Identity bits3(0) bit IX-2: Card Identity bits2(0) bit IX-1: Card Identity bits1(0) bit IX-0: Card Identity bits0(0) bit OX-3: not use (initialize to 1) bit OX-2: not use (initialize to 1) bit OX-1: not use (initialize to 1) bit OX-0: not use (initialize to 1)
TIME Slot Generator	Voice Channels Local Time Switch	Serial Voice Channel Configuration Regs. To Configure-Channel Number Assin -Source Select

DMA-Channel	DMA Controller	DMA Channels for Voice Data Transfer
DPT-I/F	4pin Modular × 2	Ch A H-L:Ch1,Ch2 Dpt Data Line Ch B H-L:Ch3,Ch4 Dpt Data Line
	ON-HOOK Condition	Always linking to PBX ext port
	OFF-HOOK Condition	Always linking to PBX ext port
	BELL Detect	receive data from PBX
	DTMF Detect	receive data from PBX
	Tone Detect	receive data from PBX

7.5. HARD DISK DRIVE

IDE interface type 3.5”

7.6. POWER SUPPLY BOARD

Power Card generates three kinds DC voltages (+5 V/-5 V, +12V), then supplies to the system. Inside the main power supply, there is a voltage maintain circuit with big capacitor. That's why DC voltage is supplied steadily, in spite of AC voltage going lower temporary. The maximum DC voltage supply period by this capacitor is 300msec.
This power source asserts DC alarm signal, when +5V DC voltage goes lower than a certain threshold level.
This signal is connected to Parallel Port inside IC301 through connector, Microprocessor can always check falling DC voltage. Power save disposition is executed when DC alarm signal assertion from power source is detected.

Table 3-5. SPECIFICATIONS OF THE POWER SUPPLY BOARD

Characteristic	Item	Specification
Input characteristics	**AC input voltage**	**AC 97 to 276V (multiple) 110 to 120V |15%, 220 to 240V |15%**
	Frequency	**47 to 63 Hz**
	Power consumption	**55W**
	Leakage current	**Less than 3 mA (division reference)**
	Inrush current	**Less than 40A**
	Efficiency	**60% (typ.)**
Noise connector voltage and noise electrical field intensity		**FCC Part 15, Subject J Class B**
		Harmonic distortion supported

Characteristic	Item	Specification
Output characteristics	+5V	
	Allowable deviation (overall fluctuation rate)	±0.25V
	Maximum	6.0A
	Minimum	0.1A
	Ripple voltage	Less than 200 mVp-p
	Ripple noise	Less than 300 mVp-p
	Overcurrent protection	Short-circuiting protection; reset by releasing the short circuit
	Variable output range	4.6 to 5.6V
	Overvoltage protection	Output voltage cut off after detection of overvoltage; reset by turning AC power back on
	-5V	
	Allowable deviation (overall fluctuation rate)	±0.25V
	Maximum	0.5A
	Minimum	0.01A
	Ripple voltage	Less than 250 mVp-p
	Ripple noise	Less than 300 mVp-p
	Overcurrent protection	Short-circuiting protection; reset by releasing the short circuit
	Variable output range	Fixed
	Overvoltage protection	None
	+12V	
	Allowable deviation (overall fluctuation rate)	±0.8V
	Maximum	0.5A (3.0A instantaneous maximum)
	Minimum	0.01A
	Ripple voltage	Less than 100 mVp-p
	Ripple noise	Less than 200 mVp-p
	Overcurrent protection	Short-circuiting protection; reset by releasing the short circuit
	Variable output range	Fixed
	Overvoltage protection	None

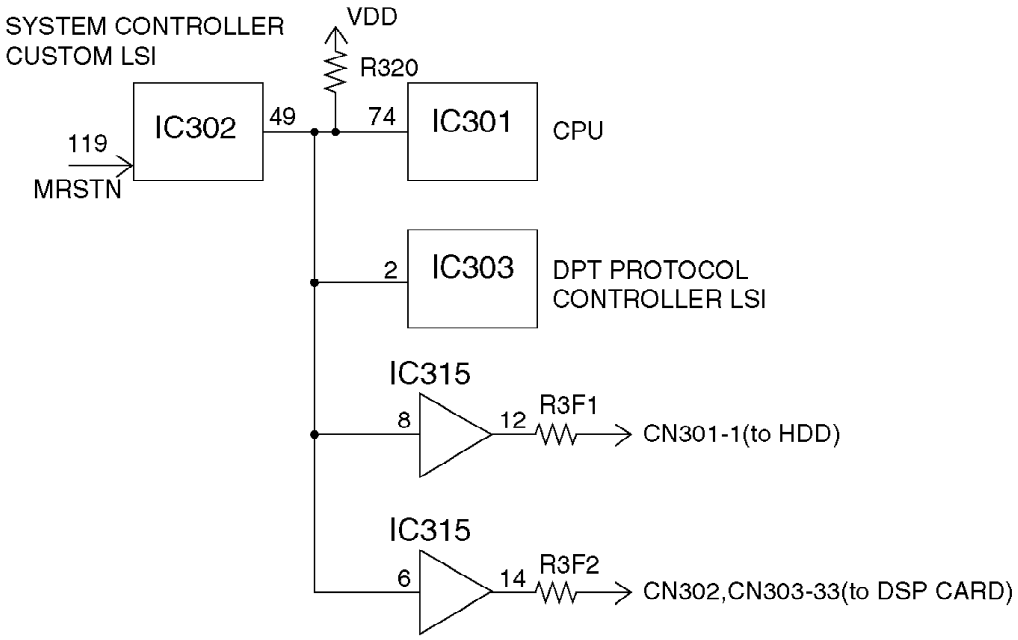
8. CIRCUIT OPERATIONS

8.1. MAIN BOARD

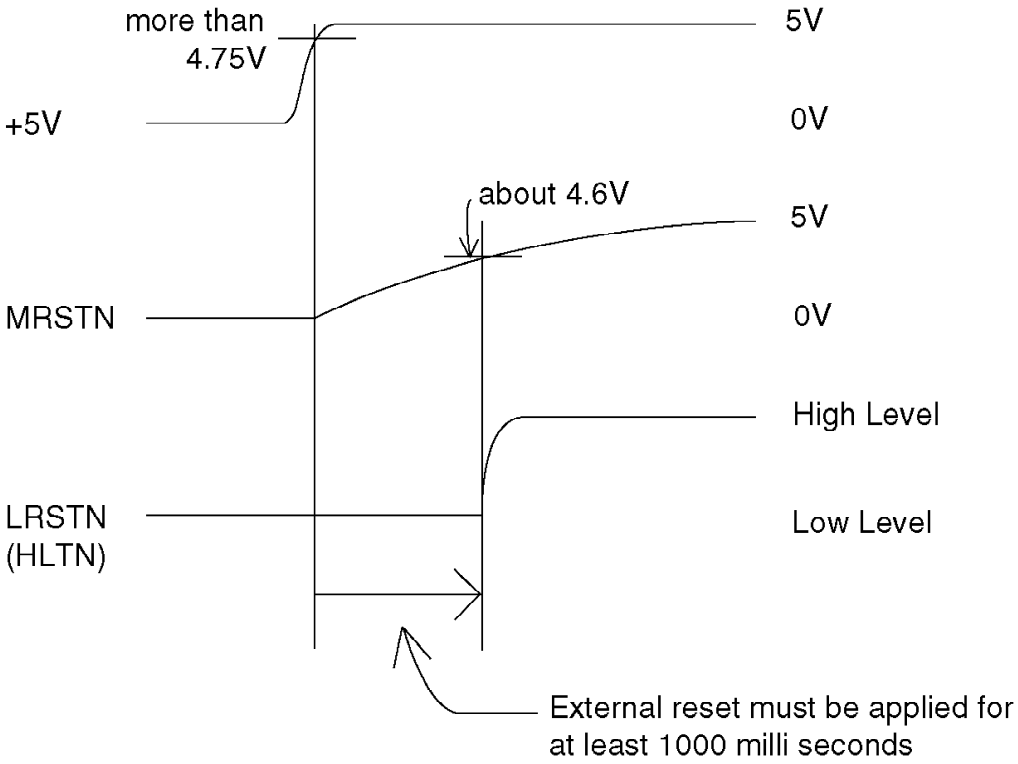
8.1.1. SYSTEM RESET (IC310)

When the power is on, the System Reset IC (IC310) initializes the whole system. MRSTN, output from IC310, is input to the RSIN (119 pin) of IC302. During RSIN's low period, IC302 is self-initialized and drives LRSTN (49 pin) and HLTN (50 pin) to low order to make the external device initialize.
LRSTN is distributed as shown below. LRSTN should be driven in High level normally. Only when the power is on, it is asserted in Low.

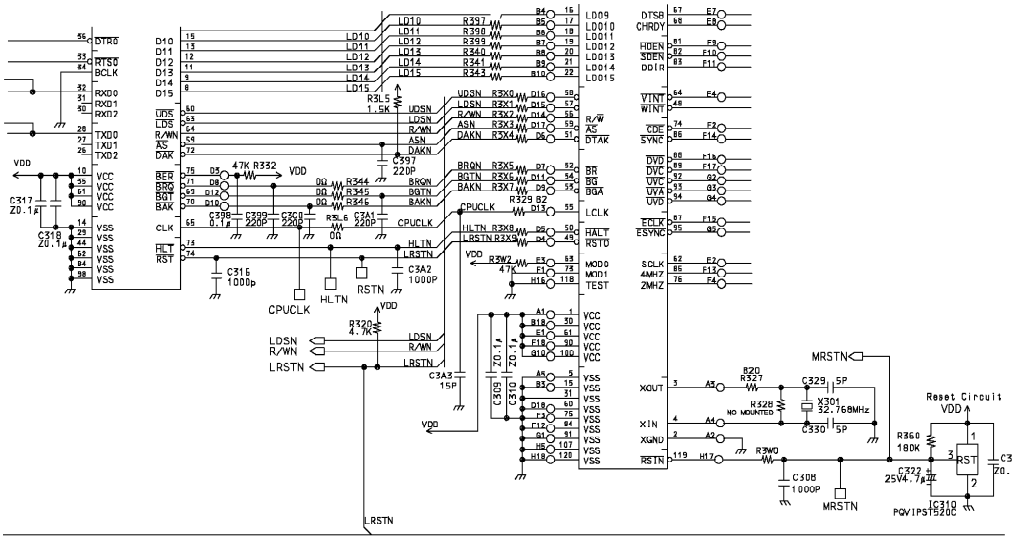
System Reset Distribution



System Reset



System Reset Signal Flow

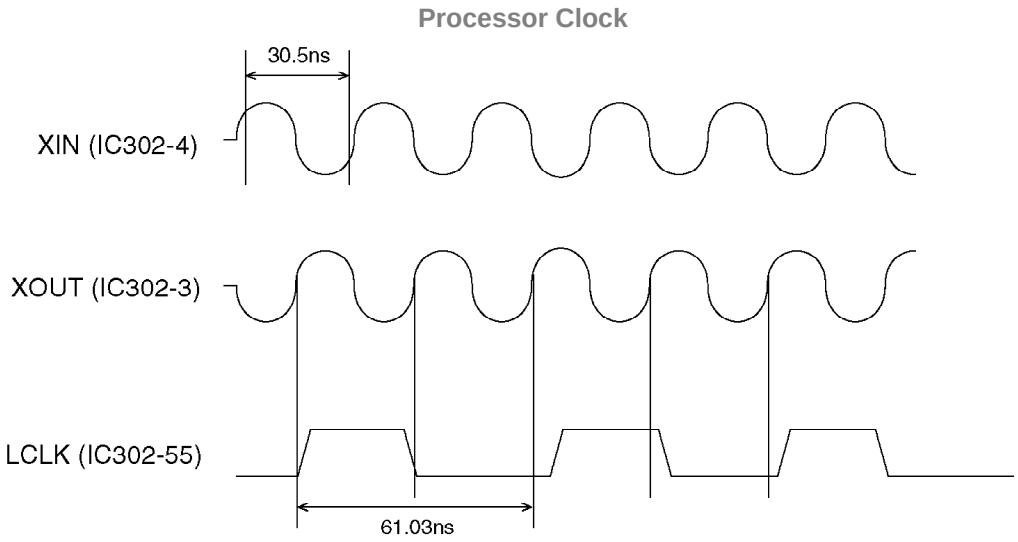


8.1.2. CPU INTERFACE (IC301, IC302)

System controller (IC302) controls the CPU (IC301) to access external resources (i.e. Memory, I/O device).

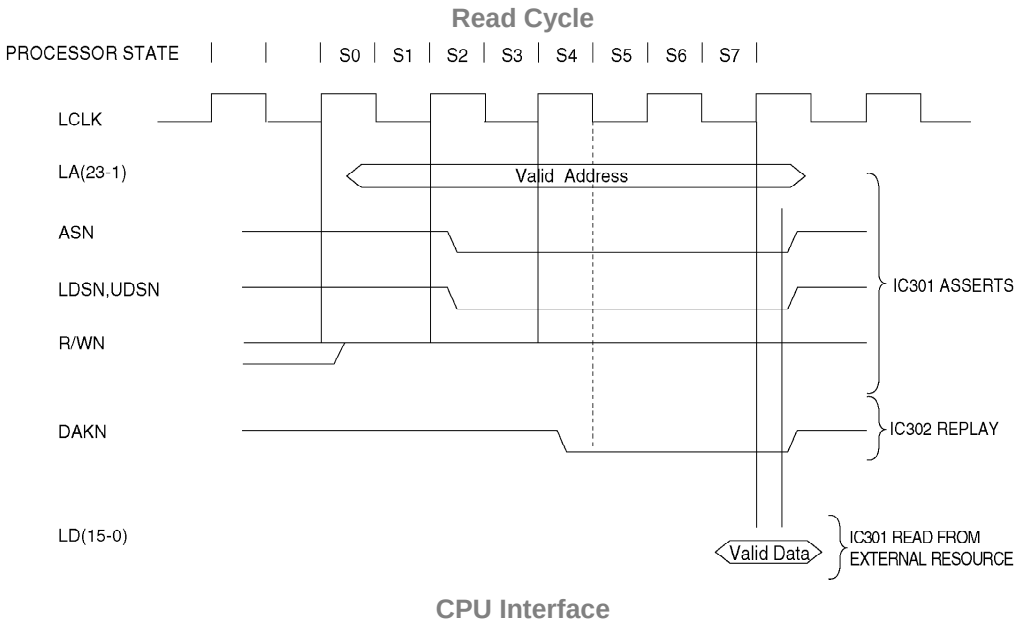
(1) Processor Clock

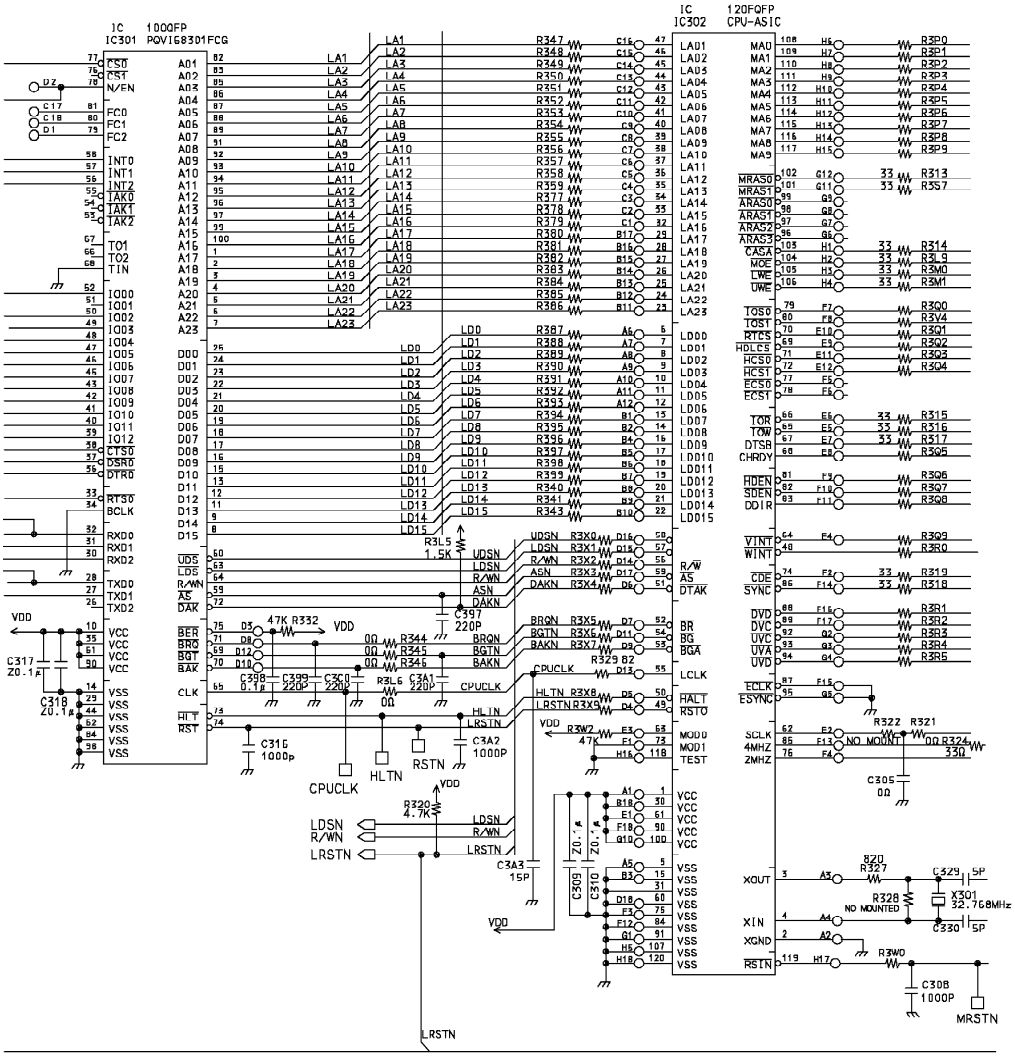
IC302 provides a processor clock from the LCLK (55) pin. Output of X'tal connected to IC302 is output from the LCLK pin divided in half inside the IC302.



(2) Read Cycle

In the read cycle IC301 outputs a valid address to A(23-1) in S0 state. Then in S2 state, IC301 asserts a signal line of ASN(59), UDSN(60), LDSN(63) and R/WM(64). IC302 decodes the condition of these signal lines and replies to DAKN(IC302-5 pin) in needed timing (normally in S4 state). By DAKN's reply, IC301 reads the valid data on the LD(15-0) line. (Refer to Processor clock).

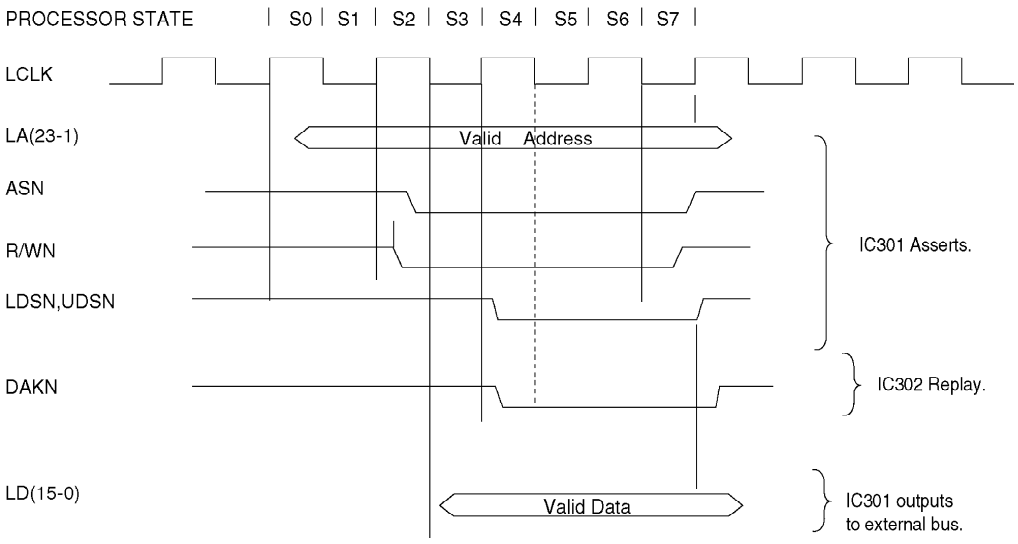




(3) Write Cycle

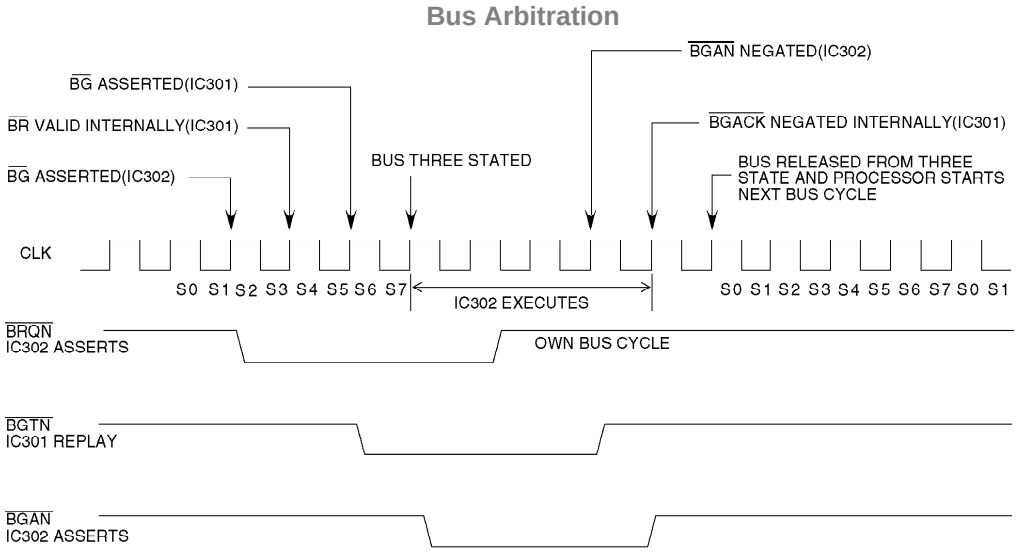
In write cycle IC301 outputs valid address to A(23-1) in S0 state. Then in S2 state, IC301 asserts a signal line ASN(59), R/WN(64). In S3 state, it outputs valid data to LD (15-0). In S4 state it asserts the signal line of UDSN(60) and LDSN (63). IC302 decodes the condition of these signal lines and replies to DAKN(IC302 - 51pin) in needed timing (normally in S4 state). IC302 terminates write cycle by the reply of DAKN. An External resource is controlled to take in effective data on LD(15-0) by a control signal generated from the system controller.

Write Cycle



(4) Bus Arbitration Cycle

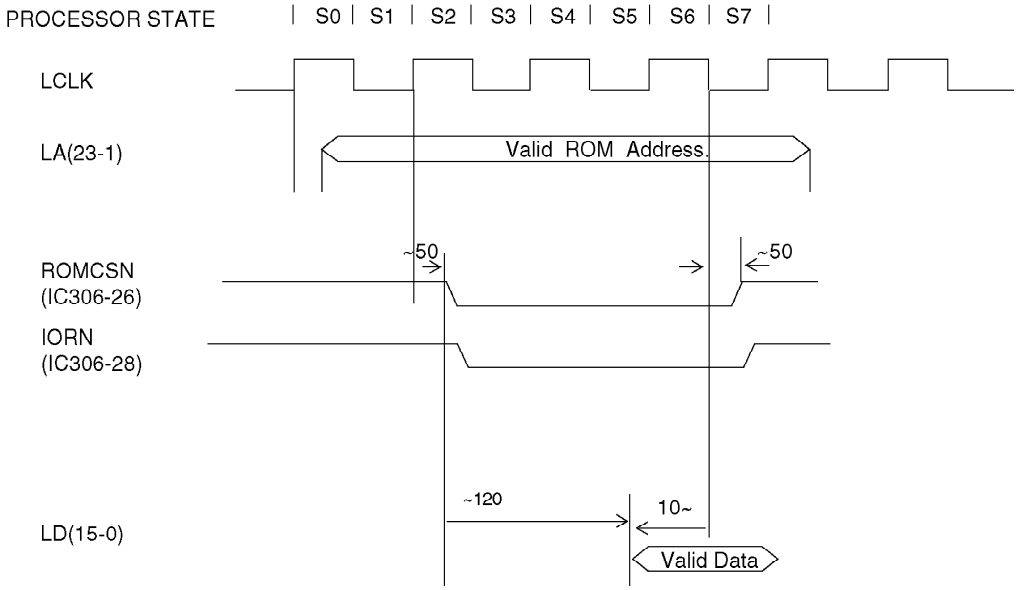
The system controller (IC302) itself should access to system memory (i.e. transfer to system memory of ADPCM Data, execution of DRAM refresh). System controller (IC302) requires the CPU (IC301) to hand over bus ownership with asserting BRQN (IC302-52 pin). When IC301 finishes its own bus cycle, it replies to BGTN (IC301 - 69) and hands over bus ownership to IC302. After detecting assertion of BGTN, IC302 asserts BAKN (IC302 - 53) then executes access to system memory for itself. At that time IC302 negates BRQN. After terminating the access to system memory, IC302 negates BGAN to hand over Bus ownership to the CPU (IC301). After detecting negation of BGAM, IC301 starts executing its own bus cycle.



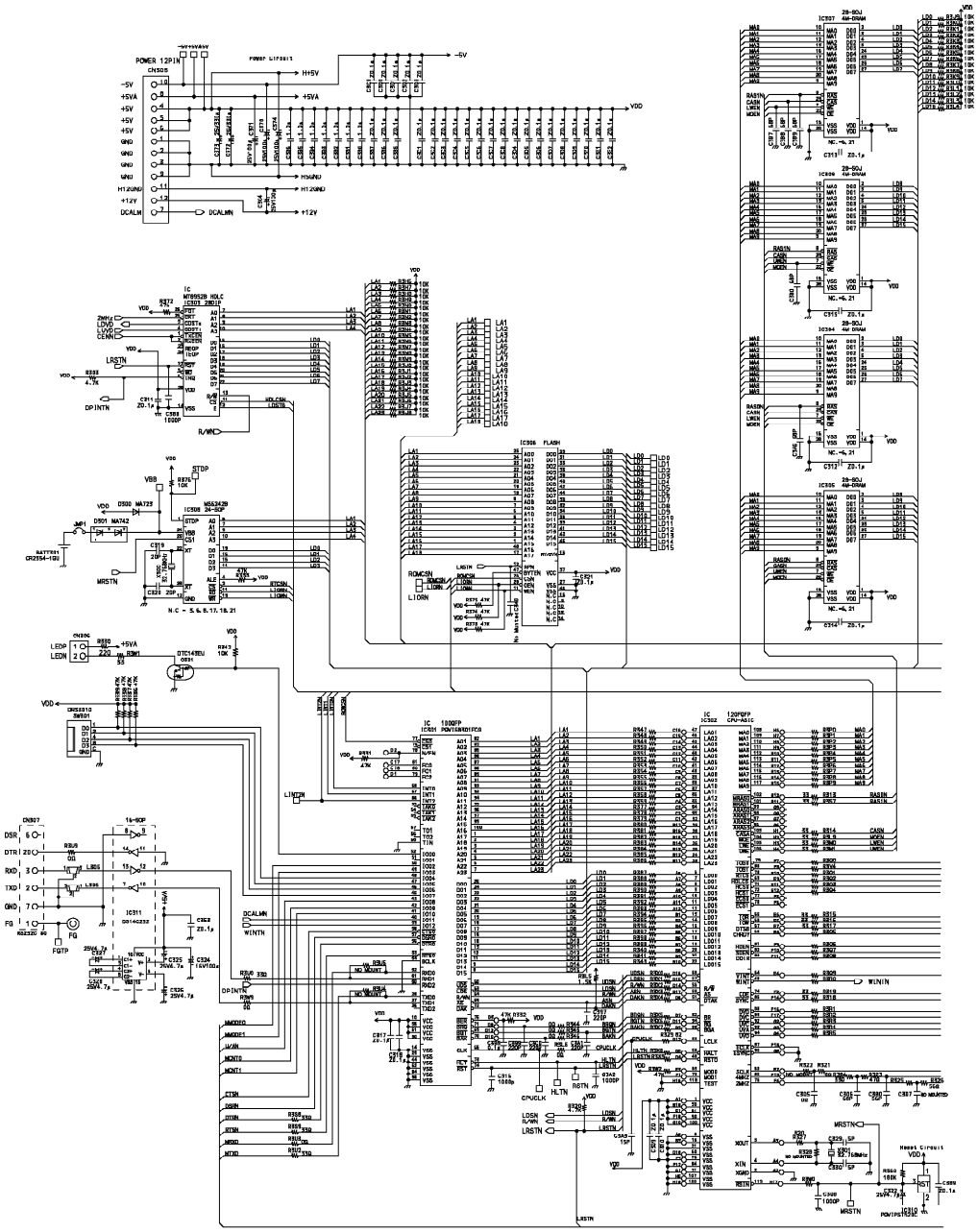
8.1.3. SYSTEM ROM (IC306)

System ROM has a program to initialize the system, diagnose itself and a loading program to load the application program from HDD to System RAM. Right after System Reset is negated, the CPU (IC301) always reads the program execution address stored in the address "00000h" of System ROM. Based on that execution address information, IC301 starts to execute program initializing inside the system of ROM.

System ROM Read



System ROM



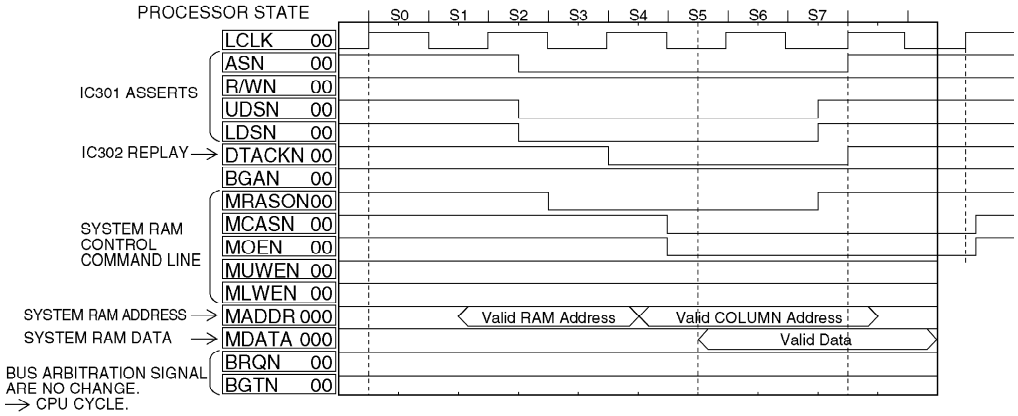
8.1.4. SYSTEM RAM (IC304, IC305,IC307 and IC309)

An Application program is loaded to system RAM by a ROM based Program. The execution program will then run on the system RAM. System RAM uses a 4Mbit Dynamic RAM. This access timing is controlled by the system controller (IC302). The operations of IC304 and IC305 are described here. The operations of IC307 and IC309 are exactly the same as those of IC304 and IC305 except that the timing of the RASIN select signal differs.

(1) System D-RAM Read Cycle by CPU

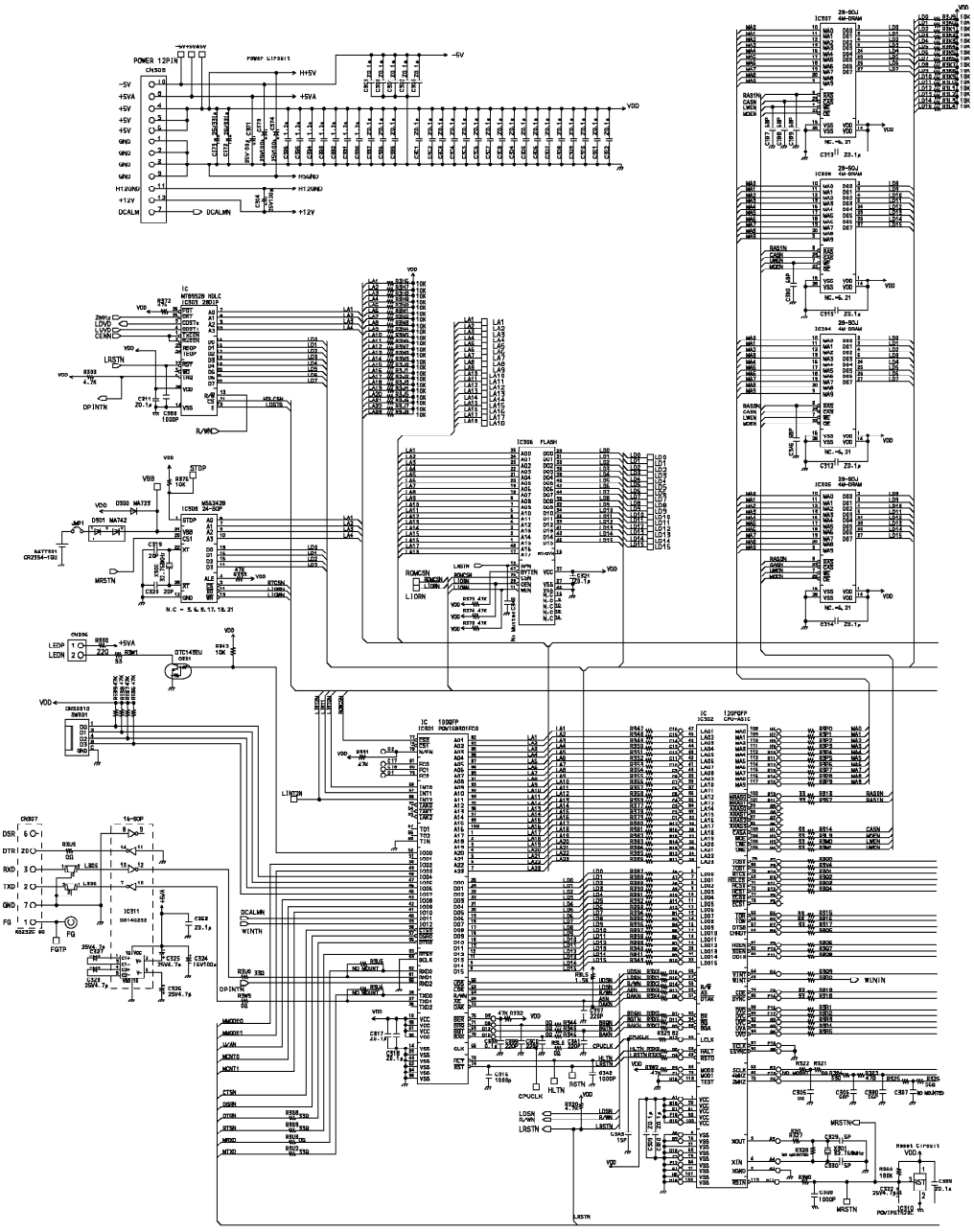
CPU executes a normal read cycle in the system RAM's Read cycle by IC301 (CPU). IC302 (System controller) decodes the condition, then generates the dynamic RAM's read signal.

System D-RAM Read Cycle by CPU



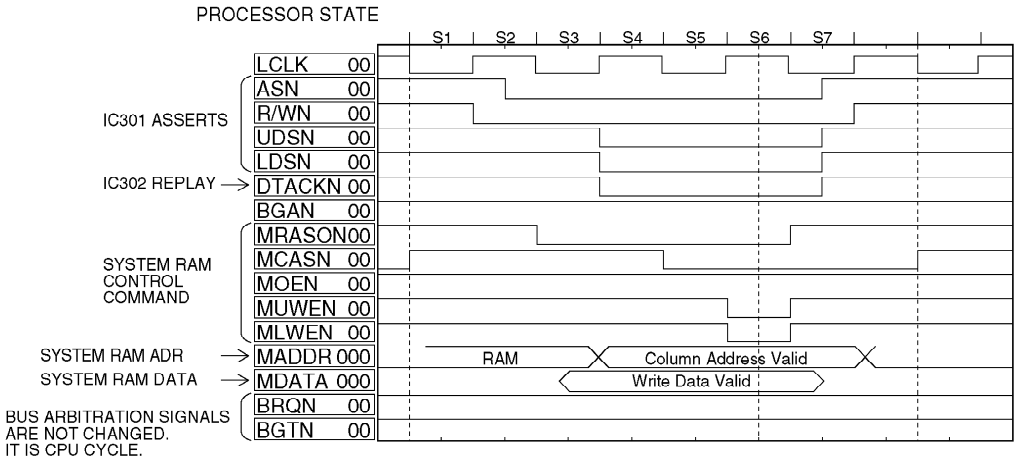
In read cycle MRASON(IC302 - 102, memory RAM address strobe) is asserted in low in the falling edge of the S2 state. IC303 and IC304 take address information on MA(9-0) in MRASON falling edge. Next MA(9-0) changes in S4 state. CASN(IC302 - 103) (Column Address Strobe) and MOEN (IC302-104) (Memory Output Enable) are asserted in low in S4 stat's falling edge. IC304 and IC305 take address information on MA(9-0) in CASN's falling edge. They output their own data to LD(15-0) because MOEN is asserted. The CPU takes effective data on LD(15-0) in S6 state falling edge.

System D-RAM



(2) System D-RAM Write Cycle by CPU

D-RAM Write Cycle by CPU



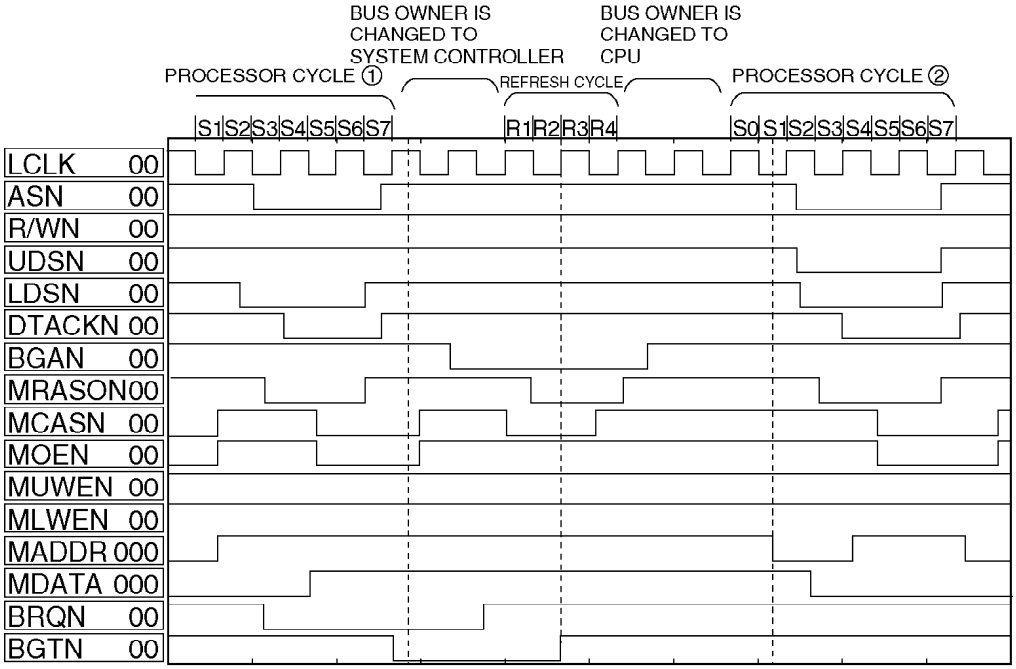
In System RAM Write Cycle by CPU, MRASON (IC302-102) = Memory RAM Address Strobe, is asserted in low in the falling edge of the S2 state. IC303 and IC304 take address information on MA(9 - 0) in the falling edge of MARASON. MA(9 - 0) varies in S4 state. CASN (Column Address Strobe) is asserted in the falling edge of S4 state. IC303 and IC304 take address information on MA(9 - 0) in the falling edge of CASN. IC301 outputs the effective data to LD(15 - 0), the period from S3 state to S6 state. IC302 asserts UWEN (106) = Upper memory write enable and LWEN (105) = Lower Memory Write Enable, in S6 state. IC303 and IC304 take the data on LD(15-0) in the falling edge of UWEN and LWEN into the inside of memory.

(3) Refresh Cycle by System Controller

In order to preserve the internal data of the Dynamic RAM used as System Memory, System Controller (IC302) executes a bus cycle, called Refresh cycle, every 16s. In order to execute the Refresh Cycle, System Controller demands Bus Ownership from CPU (IC301). After receiving bus ownership from the CPU, System Controller executes Refresh cycle. After the Refresh cycle is completed, System Controller hands over Bus Owner ship to the CPU. (Refer to 1-2. (4) Bus Arbitration Cycle). The Refresh cycle executed is called "CAS BEFORE RAS Refresh". In case of not being executed periodically, the Refresh cycle is hold in the Dynamic RAM. The Data is purged.

The Refresh cycle is executed while BGAN (IC302 - 53) is asserted, namely system controller is in the period of Bus Ownership. This cycle starts from LCLK (IC302 - 55)' s rising edge after the BGAN is asserted, then is completed during 2xLCLK. CASN (IC302 - 103) is asserted in the rising edge of R1 state. Each of them is negated in the falling edge of R3 state and in the rising edge of R4 state. Around Refresh Cycle Arbitration cycle is executed.

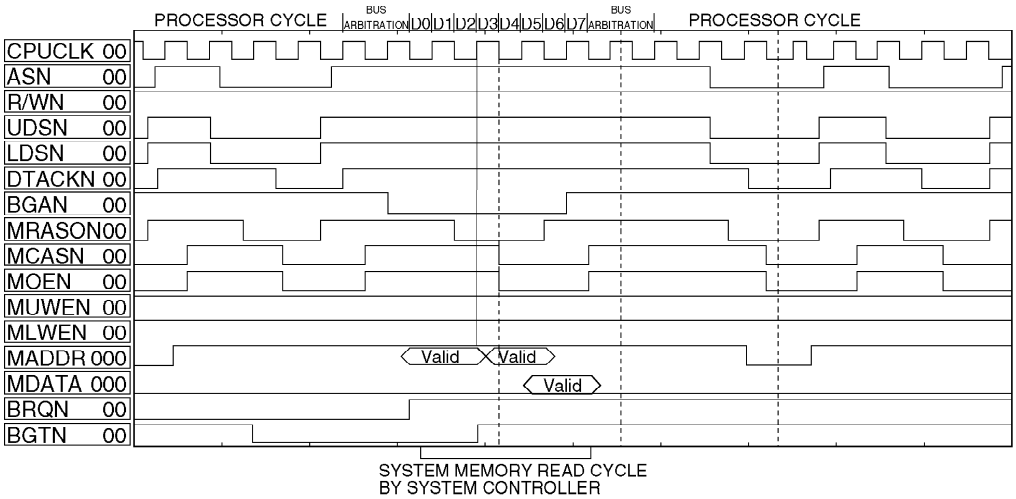
Refresh Cycle by System Controller



(4) System D-RAM Read Cycle by System Controller

In time Message Delivery to the extension line, the DSP Card requires System Controller (IC302) to send the ADPCM Data on System memory. System controller, accepting this requirement, demands Bus Ownership from the CPU (IC301). Once System controller receives Bus Ownership from the CPU, the System RAM read cycle is executed. After that System Controller hands over Bus Ownership to the CPU.

System D-RAM Read Cycle by System Controller



Once System Controller rewires Bus Ownership from the CPU, it asserts BGAN (IC302 - 53) in low and executes the System - Memory Read cycle. This read cycle starts from CPUCLK's rising/ falling edge after BGAN is asserted and ends during 4xCPUCLK.

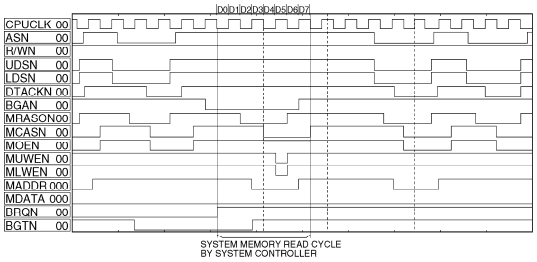
The System Controller outputs a destination address to MA(9 - 0) in D0 state. MRASON is asserted in the leading edge of D2 state and MA (9 - 0) switches over in D3 state of the leading edge. MCASN and MOEN are asserted in the leading edge of D4 state. IC303 and IC304 start outputting the data to LD (15 - 0). System controller takes in the effective data on LD(15-0) in the

leading edge of D7 state. The data taken in is sent to the DSP Card through the extension bus. In order to return bus ownership to the CPU, System controller negates BGAN in the leading edge of D7 state.

(5) System D-RAM Write Cycle by System Controller

In time Message receiving from the extension line, ADPCM data generated by the DSP is added to the system RAM address information of where to transfer the DSP card. Then ADPCM data is sent to the system controller. Receiving this information, System Controller requires the CPU to hand over Bus ownership in order to write designated addresses. By this requirement, system controller obtained bus ownership executed by the System Ram Write cycle.

System D-RAM Write Cycle by System Controller



In Write cycle by System Controller, the output timing of MRASON, MA(9 - 0) and MCASN are the same as the Read cycle. In Write cycle MOEN is not asserted, and MUWEN and MLWEN are asserted in D5 state. In time, BGAN is asserted in low, System Controller outputs effective data to LD (5 - 0). This effective data is stored in IC303 and IC304 at the falling edge of MUWEN and MLWEN.

8.1.5. SYSTEM PORT

The System Port Function is provided by PIO (Parallel Input Output Control) inside IC301. System Port's functions are

- **to control the Power Indicator (LED)'s ON/OFF**
- **to read the condition of the DIP switch**
- **to read the condition of DCARM (DC Alarm) input from the Power Supply Board**
- **Forced Modem Reset (MDRSTN)**

(1) Power Indicator (LED) ON/OFF control

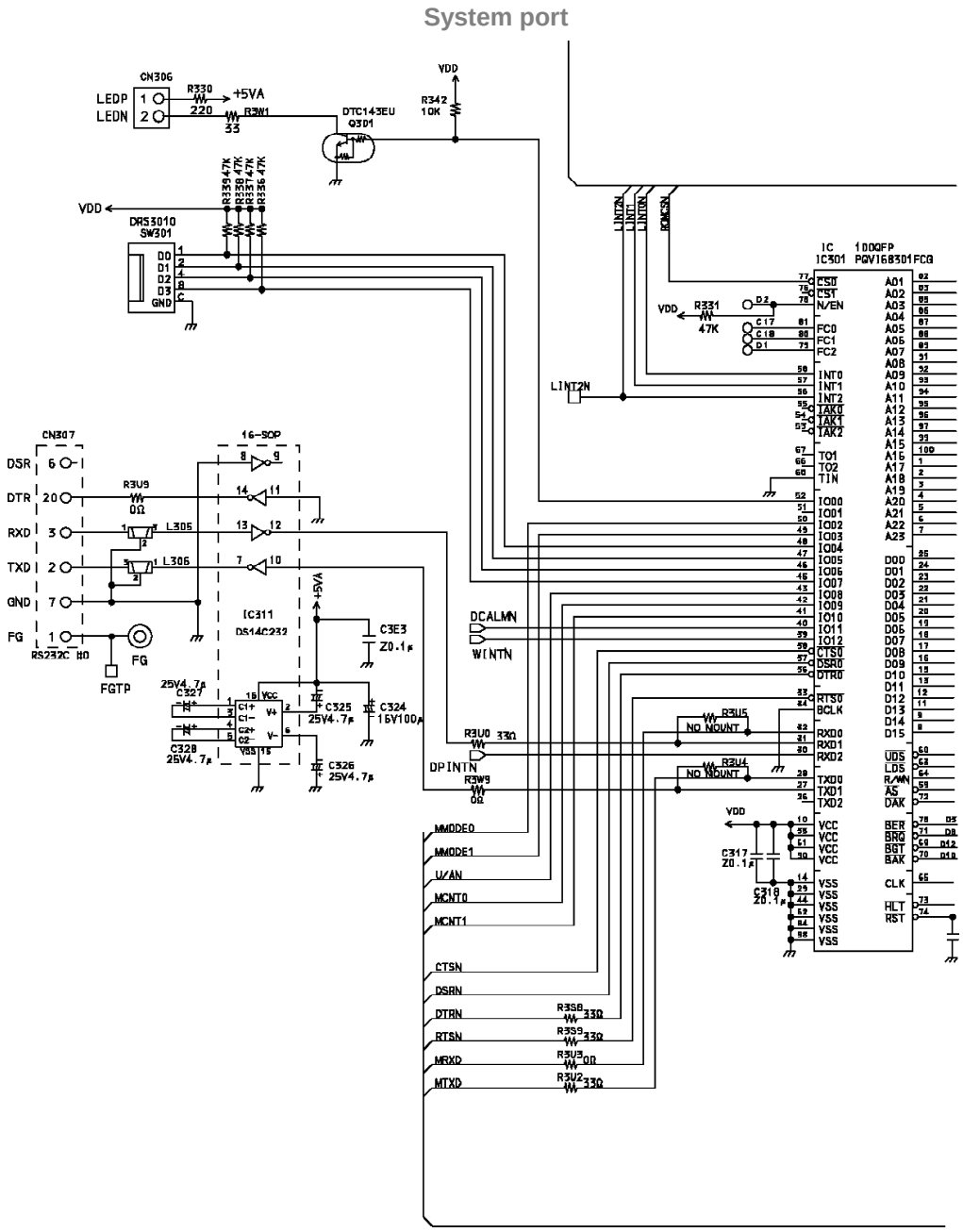
The Power Indicator (LED)'s ON/OFF is controlled by IC301 - pin 52. This pin is connected to the base of the digital transistor Q301. When IC301 - pin 52 is "High", between the emitter and collector of Q301, it becomes transmissible and LED turns on. When IC301 - pin 52 is "Low", between emitter and collector of Q301, it becomes non-transmissible and LED turns off.

(2) DIP switch port

The Rotary switch is surrounded by IC301 - pin 45 ~ pin 48.

(3) DC ALARM PORT

When Power Supply Board detects low DC voltage, it drives the CN 305 - 5 pin to low, then informs the Main Board of the DC power condition. The input signal from CN305 - pin 5 is taken as DCALMN from the IC301-pin 40. This signal normally is "High".



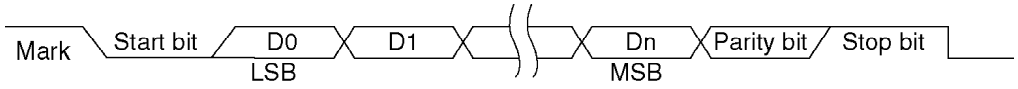
8.1.6. RS-232C INTERFACE

The RS-232C interface is provided by SIO (Serial Input Output Controller) built-in the IC301.

(1) Data Format

When a data character to be transmitted is placed in the SIO, the serial interface automatically adds one start bit before the data bits (lower order bits are output first) and the specified number of stop bits after the data bits. When parity (even, odd) is specified in the mode register, a parity bit is inserted before the stop bit.

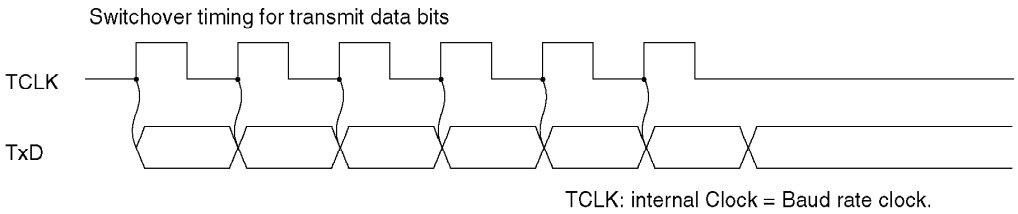
Data Frame



(2) Data Transmission

The CPU checks the DSR (IC301 - 57): Data Set Ready is low, i.e. terminal side's preparation for receiving data finishes, then starts transmission. After transmitting the start bit, the transmit controller automatically appends a parity bit and stop bit to the data character of the specified length and shifts these out to the TxD line. When the next data character has been written to the transmit data buffer, transmission continues with the start bit of the next data character following the stop bit of the current data.

Switchover Timing for Transmit Data Bits

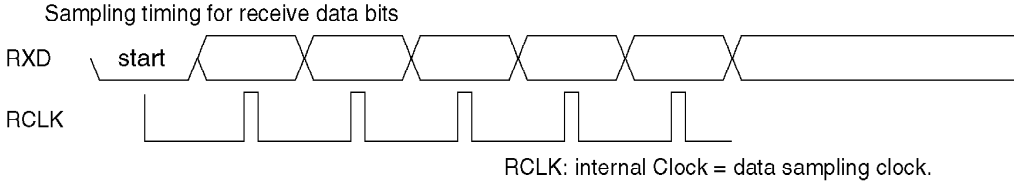


(3) Data Reception

The RxD line is high when no data is in it (mark status). The beginning of a start bit is detected when the input goes low.

For receiving, the first low sampled RXD is detected and, if the sampled data are low for four internal CLKs, this low level is considered to be a valid start bit. The center point of the following data bits is then determined and each data bit is sampled on the TCLK falling edge.

Switchover Timing for Receive Data Bits

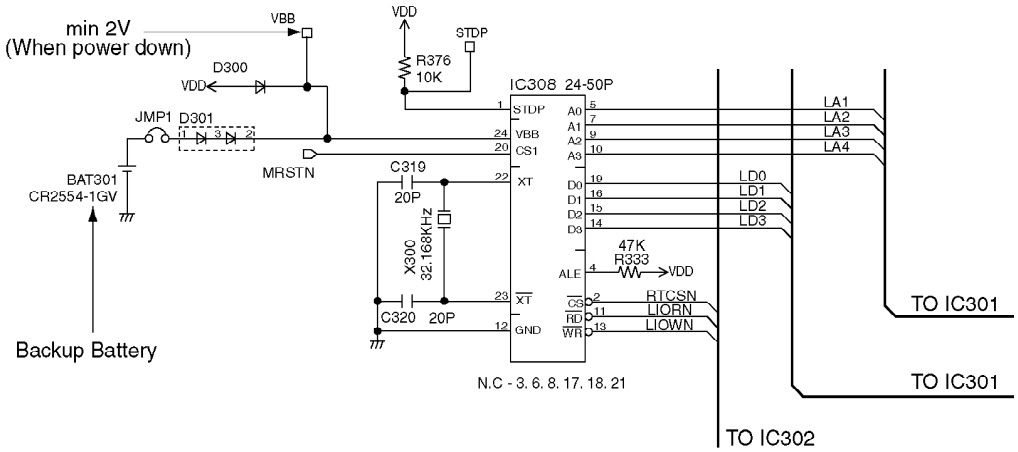


(4) RS-232C Transceiver (IC311)

The IC311 is a transceiver IC only for RS-232C. IC311 possesses a built-in DC/DC Converter and generates ±10 V needed for the RS-232C interface. Each terminal voltage of the DC/DC converter block is in system port.

8.1.7. REAL TIME CLOCK

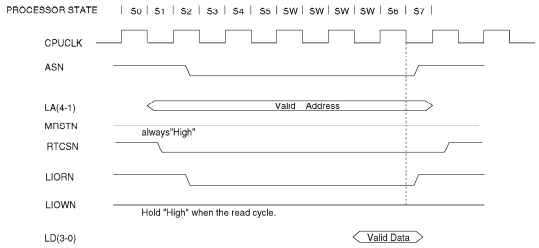
Real Time Clock



The Real Time Clock is provided by IC308. IC308 is a Real Time Clock IC with a fail-safe calendar to be able to read and write from seconds. To interface with the CPU four data buses=(LD<3-0>), four address buses=(LA<4-1>), two control buses (LIORN, LIOWN) and two chip select (RTCSN, MRSTN) are needed for set the time/modification/read out.

(1) CPU Read Cycle

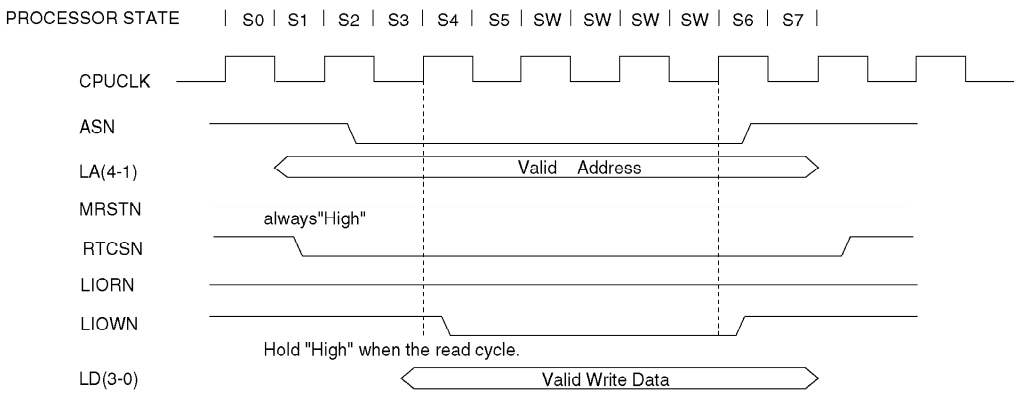
Real Timing Clock Read CPU



The CPU (IC301) outputs valid Address to LA(4-1) in S1 state. System Controller (IC302) asserts RTCSN in low. System Controller asserts LIORN to low in S2 state. To respond to low assertion of LIORN, the IC308 outputs the internal register corresponding with LA (4 - 1). At that time to LD (3 - 0) the CPU takes in effective data on LD (3 - 0) in the falling edge of S6 state.

(2) CPU Write Cycle

Real Time Clock Write Cycle by CPU

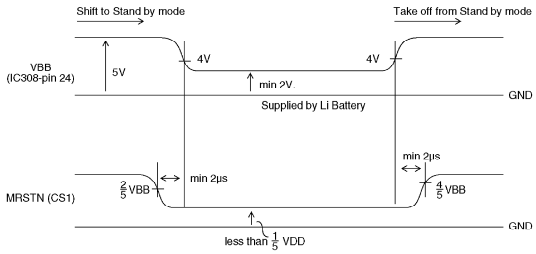


The CPU (IC301) outputs Valid Address to LA (4 - 1) in S1 State. System Controller (IC302) asserts RTCSN in low. The CPU outputs Valid Write Data to LD (3 - 0) in S3 state. System Controller asserts in low in time from the rising edge of S4 state to the rising edge of S6 state. IC 308 takes the effective data on LD (3 - 0) in the rising edge of LIOWN.

(3) Battery Back Up Interface

IC308 has two modes: operation mode and standby mode. Operation mode is guaranteed the interface with CPU and is the condition to be able to setting time/modification/read and write. If provided more than 4/5 of VDD voltage is relayed to the CS1 terminal (pin 20), it becomes the operation mode. If less than 1/5 of VDD voltage is relayed to the CS1 terminal (pin 20), it becomes the stand-by mode. By IC308 checking time function inside IC works but the interface with CPU is not guaranteed. In this mode the consumption of the current decreases. In order to switch over these two modes (operation mode and stand-by mode), The MRSTN signal is connected to the IC308 CS1 terminal.

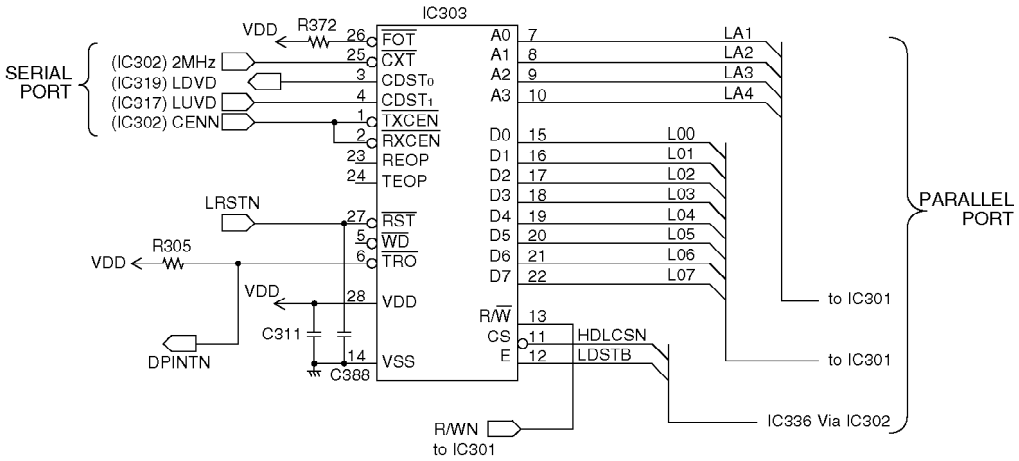
Battery Backup



When Power goes down, MRSTN signal changes the level lower than 2/5 VBB before VBB reaches at 4V. When Power goes up, MRSTN signal changes the level higher than 4/5 VBB after VBB reaches at 4V. With this MRSTN signal, a certain switch over (operation mode and stand-by mode) is guaranteed. In order to guarantee the checking time function of IC308 in stand-by mode, more than 2V voltage should be added to VBB.
This guaranteed voltage is supplied by the lithium battery.

8.1.8. DPT PROTOCOL CONTROLLER

DPT Protocol Controller Interface



When Panasonic KX-TD series PBX and VPS are connected, VPS adopts a Data Format and communication protocol based on X.25 (CCITT) level 2 in order to exchange its own status and command parties between the VPS and PBX mutually. This data communication is provided by IC303.

The DPT Protocol Controller has two ports. The serial port transmits and receives formatted data packets and the parallel port provides a CPU interface for access to various registers in the Protocol Controller.

The CPU Port allows parallel data transfers between the Protocol Controller and a CPU bus. This interface consists of Data Bus (LD7 - LD0), Address Bus (LA4 - LA1), Data Strobe (LDSTB), Chip Select (HDLCSN) and Read/Write Control (R/WN). The CPU can read and write to various registers in the Protocol Controller. The DPINTN, active Low output indicates and interrupt requests to CPU. The interrupt request will be asserted when the packet data transmission is complete or four more packet data receptions are confirmed.

The serial port handles bit oriented protocol structure and formats the data as per the packet switching protocol defined in the X.25 (level 2) recommendations of the CCITT. It transmits and receives the packet data (information or control) serially as shown in Figure 4-12.

DPT Data Packet Format

FLAG	DATA FIELD	FCS	FLAG
1 Byte	N Byte (n ≦ 2)	2 Byte	1 Byte

Flag:

The flag is a unique pattern of 8 bits (01111110) which defines the frame boundary. The transmit section generates the flags and automatically appends them to the frame to be transmitted. The receive section searches the incoming packets for flags on a bit-by-bit basis and establishes frame synchronization. The flags are used only to identify and synchronize the received frame.

Data:

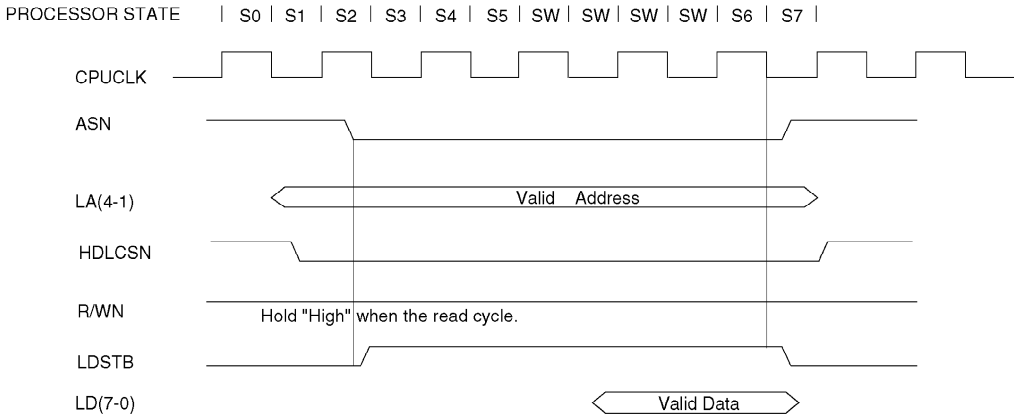
The data field refers to the Address, Control and Information fields defined in the CCITT recommendations. A valid frame should have a data field of at least 16 bit.

Frame Check Sequence (FCS):
The 16 bits following the data field are the frame check sequence bits. The generator polynomial is:
G(x) = x16 + x12 + x5 + 1
The transmitter calculates the FCS on all bits of the data field and transmits after the data field and before the end flag. The receiver performs a similar computation on all bits of the received data and FCS fields. The result is compared with FOB8Hex. If it matches, the received data is assumed to be error free.

Zero Insertion and Deletion:
The Protocol Controller, while sending either data or the 16 bits FCS, checks the transmission on a bit-by-bit basis and inserts a ZERO after every sequence of five contiguous ONEs (including the last five bits of FCS). This ensures that the flag sequence is not simulated. Similarly, the receiver examines the incoming frame content and discards any ZERO directly following the five continuous ONEs.
In the serial port, the formatted data packets are shifted in/out serially at a rate equal to the clock frequency of 2 MHz. The LDVD output is transmitted on the rising edge and the receiver samples the LUVD input on the falling edge of the clock. The CENN controls have effect only after the current bit in the packet is transmitted/received.

(1) CPU Read Cycle

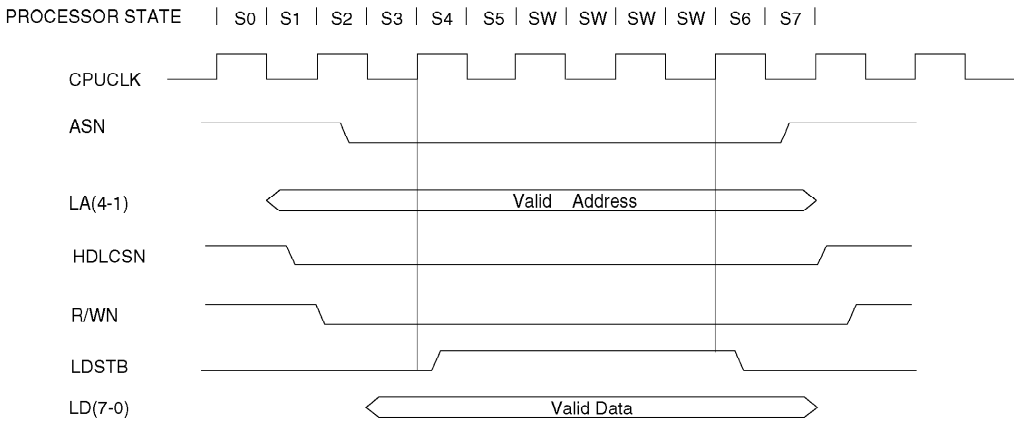
DPT Protocol Controller Read Cycle by CPU



CPU (IC301) outputs Valid Address to LA(4 - 1) in S1 state while holding R/WN High. System Controller (IC302) asserts HDLCSN in Low. System Controller asserts LDSTB High in S2 state. LDSTB is asserted in High, R/WN is in High = read condition, IC303 outputs the condition of internal register corresponds with LA (4 - 1) at that time to LD (7 - 0). CPU takes in effective data on LD(7 - 0) in the falling edge of S6 state.

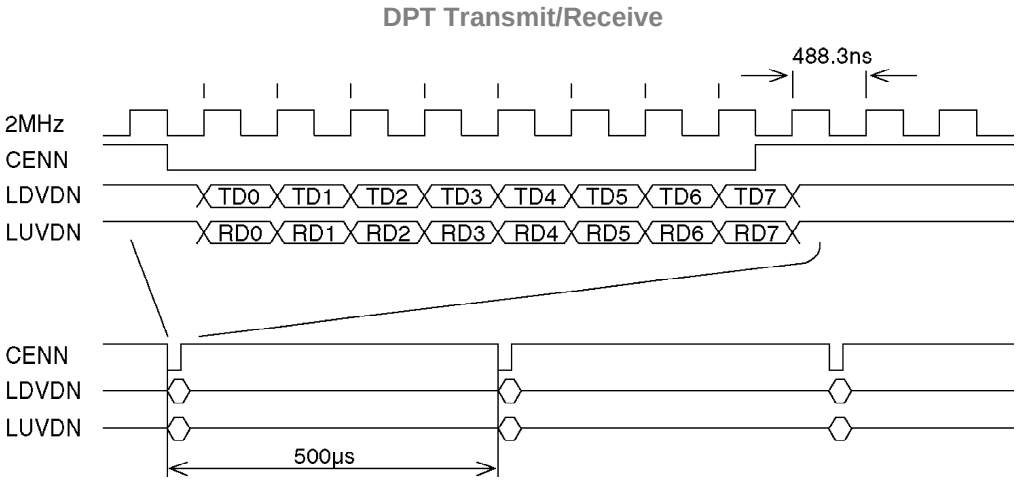
(2) CPU Write Cycle

DPT Protocol Controller Write Cycle by CPU



CPU (IC301) outputs Valid Address to LA(4 - 1) in S1 state. System Controller (IC302) asserts HDLCSN in Low. CPU asserts R/WN in Low = Write in S2 state, then from S3 state it outputs an effective data to LD (7 - 0). System Controller asserts from the period of the rising edge in S4 state to the rising edge of S6 state LDSTB High. IC303 takes in the condition of LA (4 - 1) in the rising edge of LDSTB and writes on the internal register effective data corresponds with LA (4 - 1) internal register in the falling edge of LDSTB.

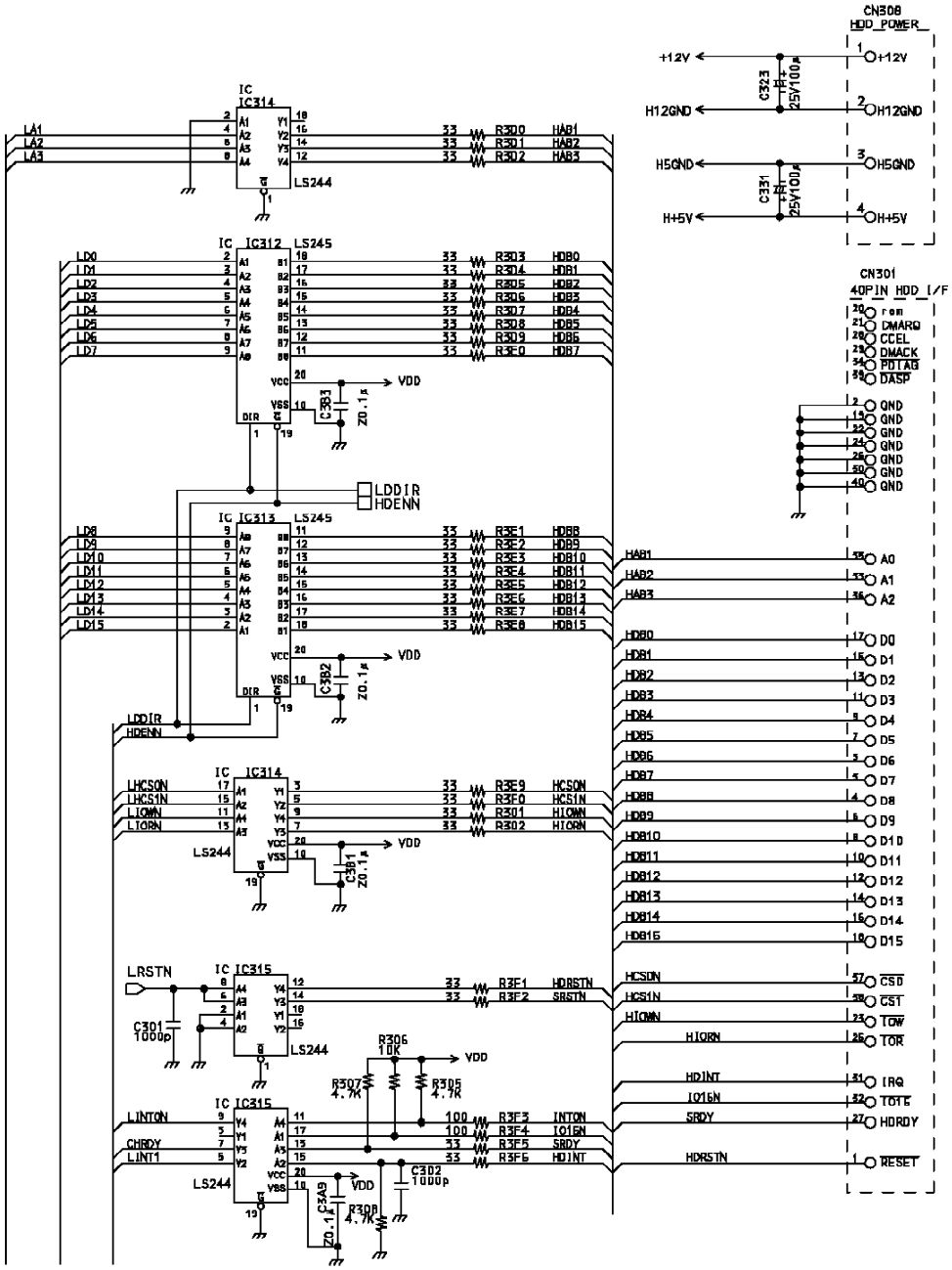
(3) DPT Transmit/Receive Timing



DPT transmit data (LDVDN) shifted out from IC303 in the rising edge of 2MHz is sent out though IC319 to the DSP card. DPT reception data (LUVDN) input from the DSP card is input though IC319 to IC303, then sampled in the falling edge of 2MHz. While an effective DPT data exists on the signal line of LDVDN and LUVDN, CENN is asserted in low by the System Controller (IC302). CENN is asserted by system Controller in the falling edge of 2MHz, and negated in the falling edge after 8 clock cycles. IC303 shifts out effective transmit data to LDVDN in the rising edge of 2MHz. Effective transmit data is from the rising edge of 2MHz right after CENN is asserted to the rising edge right after CENN is negated. Moreover, IC303 samples an effective reception data from the falling edge of 2MHz right after CENN is asserted to the falling edge right after CENN is negated on LUVDN in the falling edge of 2MHz. Data Packet is input and output every 8 bits to the Protocol Controller. The cycle is 500 μ s.

8.1.9. HARD DISK INTERFACE

Hard Disk Interface



The Hard Disk Drive used in the VPS installs an intelligent interface built-in disk controller. Main Board's Interface circuit is shown in Hard Disc Interface. The Hard Disk interface allows parallel data to transfer between the Hard Disk Drive and a CPU bus. This interface consists of a Data Bus (D15 - D0), Address Bus (A2 - A0), Chip Select (CS0, CS1) and 6 control signals (IOR, IOW, IRQ, IO16, HDRDY, RESET). The VPS does not use HDRDY and IO16 signals. The Hard Disk Interface Connector's pin Assignment is shown below.

Hard Disk interface Pin Assignment

Pin No.	Signal Name	Pin No.	Signal Name
01	-HOST RESET	02	GND
03	+HOST DATA 7	04	+HOST DATA 8
05	+HOST DATA 6	06	+HOST DATA 9
07	+HOST DATA 5	08	+HOST DATA 10
09	+HOST DATA 4	10	+HOST DATA 11
11	+HOST DATA 3	12	+HOST DATA 12
13	+HOST DATA 2	14	+HOST DATA 13
15	+HOST DATA 1	16	+HOST DATA 14
17	+HOST DATA 0	18	+HOST DATA 15
19	GND	20	KEY
21	+DMARQ	22	GND
23	-HOST IOW	24	GND
25	-HOST IOR	26	GND
27	+IOCHRDY	28	+CSEL
29	-DMACK	30	GND
31	+HOST IRQ14	32	+HOST IO16
33	+ADDR1	34	+HOST PDIAG
35	+ADDR0	36	+ADDR2
37	-HOST CR0	38	-HOST CR1
39	-DAST	40	GND

(1) Hard Disk Interface Signals Descriptions

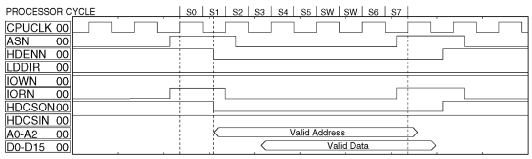
Signal Name	Pin No.	Input/ Output	Explanation
-RESET	1	O	Reset signal from host system. Power source of host system turns on, becomes active.
GND	2, 19, 22, 24, 26, 30, 40, 43	O	Ground
DATA 0 - 15	3 - 18	O	16 bit mutual direction data bus. Low-ranking 8 bit (DATA 0 - transferred when it gains access to registers except for the register and ECC data inside the data register.
KEY Pin	20		Key pin to prevent cable connector from incorrect insertion. drive side is broken off and removed, then inserted in the pi cable side.
-10W	23	O	Write strobe signal. When drive select signal (-CS0.1) is acti data bus is written in the register inside drive by the Trailing
-10R	25	O	Read strobe signal. When drive select signal (-CS0.1) is acti inside the register is output onto the data bus with low activ is read into the host system with Trailing Edge.

Signal Name	Pin No.	Input/ Output	Explanation
IRQ	31	I	Interrupt signal to host system. It is active when drive is sele IEN (Interrupt Enable) inside flexed disk register is active. Ge interrupt phenomenon or not it becomes high- impedance st except when the above condition occurs. IRQ signal is reset host system reads status register or command is written in t command register.
RESERVED	21, 27, 28, 29, 44		Reserve Signal. Non-connecting condition.
-IO16	32	I	The signal (Open drain) informs the 16 bit data transferred m bit data register is gained access). (Not used)
-PDIAG	34	I/O	Used to inform master drive of the existence of slave drive a receive and send the result of the diagnostic command betw master and slave drive. (Not used)
A0, A1, A2	33, 35, 36	O	Address decode signal of internal register.
-CS0	37	O	Chip select signal. To select one group within two internal re groups.
-CS1	38	O	Chip select signal. To select one group within two internal re groups.
-DASP	39	I	During drive access (from receiving command to command becomes active. Used to drive external LED. Composing Master/slave, it is used to inform master drive of existence of the slave drive. (Not used)
+5V (LOGIC)	41	O	Power source of logic group - analog group
+5V (MOTOR)	42	O	Power source of motor driving.

*** The signal from drive to host system is I (Input), from host system to drive is O (output).**

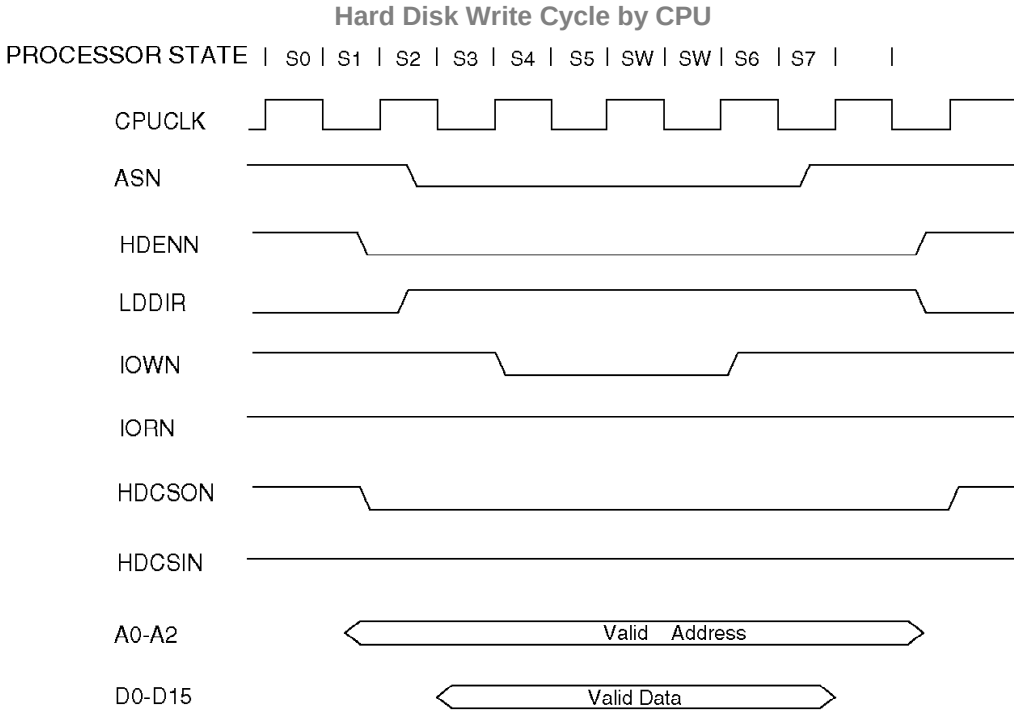
(2) CPU Read Cycle

Hard Disk Read Cycle by CPU



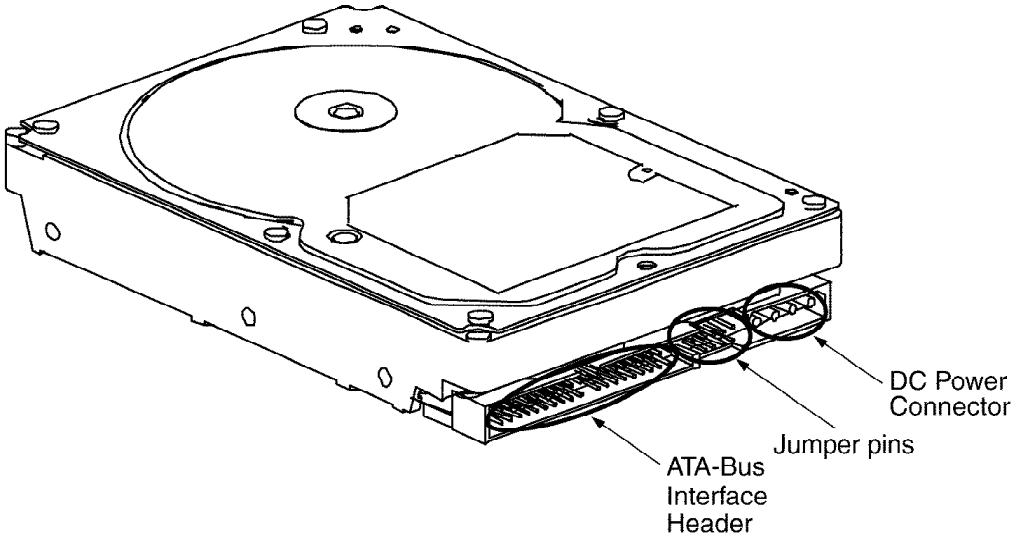
CPU (IC301) outputs Valid Address to A(2 - 0) in S1 State. System Controller (IC302) asserts either HDCSON or HDCSIN. System Controller asserts IORN low in S2 state. Hard Disk outputs the condition of internal register correspondence with A(2 - 0) IORN in time IORN is asserted to D(0 - 15). The CPU takes effective data on D(15 - 0) in the falling edge of S6 State. In Read Cycle, IC312/IC313 (L5245 Bus Transceiver) is the Control Signal. HDENN (IC312/IC313, pin 19) is asserted in low in the period from S1 state to S7 state. LDDIR (IC312/IC313, pin 1) is asserted in low.

(3) CPU Write Cycle

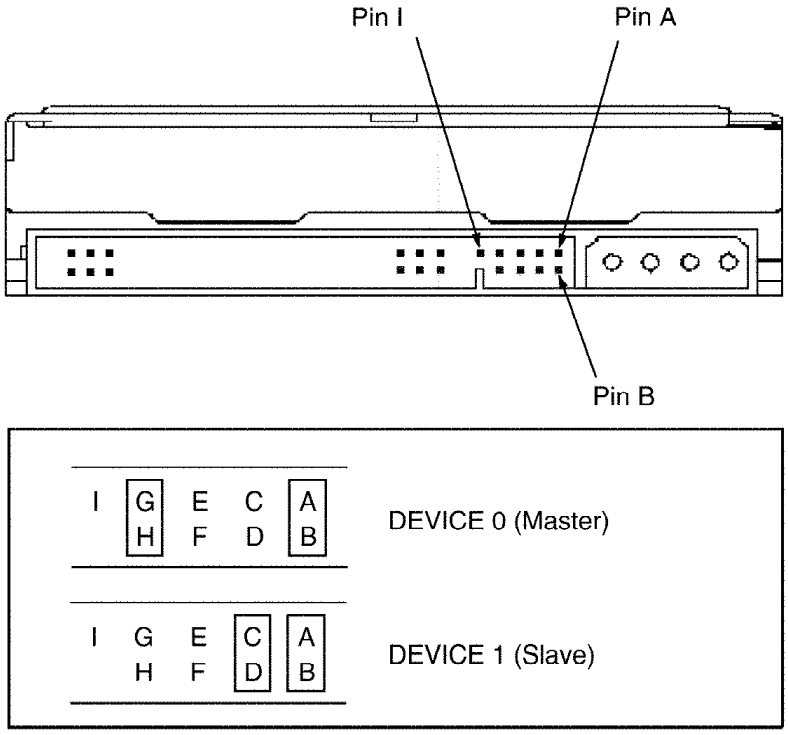


CPU (IC301) outputs Valid Address to A(2 - 0) in S1 State. System Controller (IC302) asserts either HDCSON or HDCSIN. CPU outputs effective written data onto D(15 - 0) in the period from S3 state to S7 state. System Controller is asserted in low in the period from the rising edge of S4 state to rising edge of S6 state. Hard Disk takes effective data on D(15 - 0) inside by the rising edge of IOWN. In Write Cycle HDENN(IC312/IC313 - pin 19), Control Signal of IC312/IC313 (LS245 Bus Transceiver), is asserted in low in the period from S1 state to S7 state. LDDIR (IC312/IC313 - pin 1) is asserted in low in the period from S2 state to S7 state.

(4) Setting the Drive's Jumpers (IBM Deskstar 60GXP)



Jumper Locations for the IBM Deskstar 60GXP Hard Disk Drive



Jumper Locations on the Interface Connector

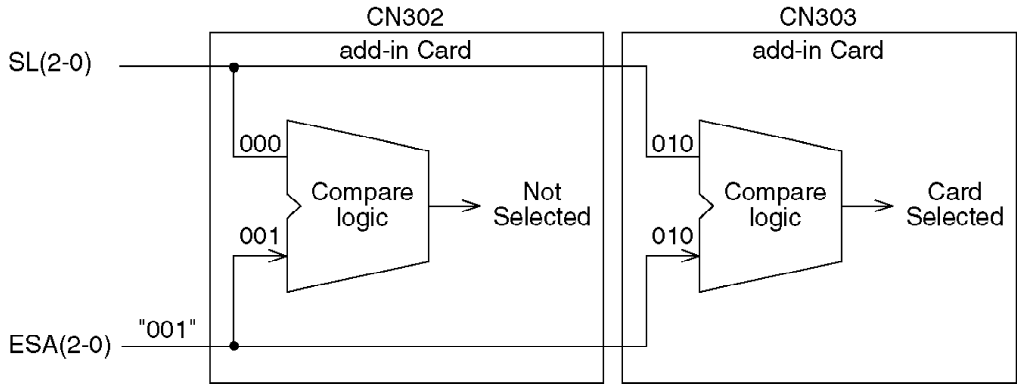
Note:
HDD is subject to change without notice. For Jumper setting of HDD, refer to HDD makers' homepages and so on.

8.1.10. EXTENSION BUS (DSP CARD INTERFACE)

The Expansion Bus has two ports. The serial port transmits and receives the voice data and the parallel port provides a CPU interface for access to various registers in the add-in card. The Main Board distributes the Bus signals to 2 expansion connectors (CN302, CN303).

(1) Add in Card Selection Signals

The Main Board provides these connectors Slot ID Signal composed by S (2 - 0). SL (2 - 0) is used in case of gaining access to add-in Card mounted by Expansion Connector, to select a card from others. The Add-in Card mounted to Expansion Connector compares the value of SL (2 - 0) provided from the connector with a part of destination address = ESA (2 - 0) provided by Microprocessor. The result of the comparison is considered by the add-in card condition of card selected. In this VPS, "000" for CN302 = slot 1 and "010" for CN303 = slot 2 = slot 2 are provided.

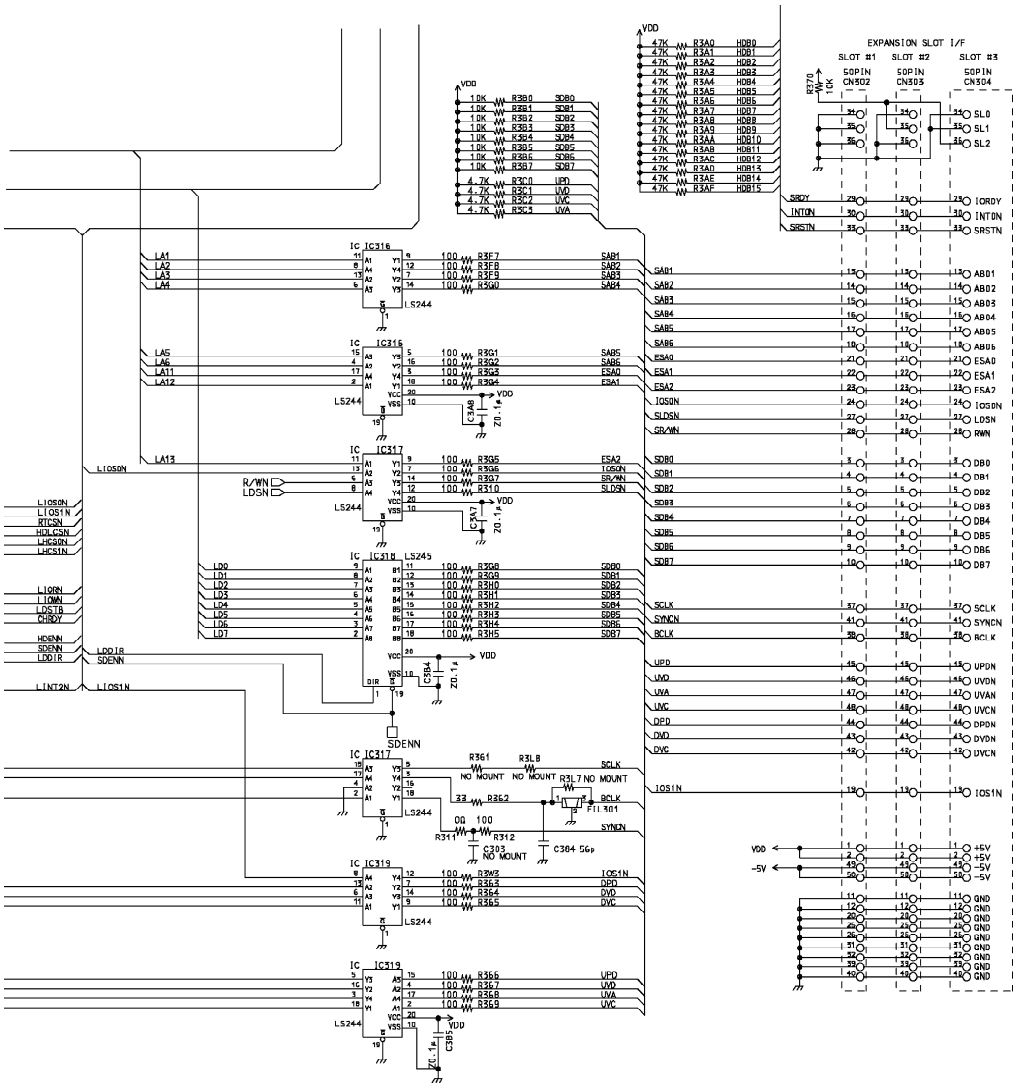


(2) CPU Port

The CPU Port allows 8 bit parallel data transfers between the various registers on the add-in card and a CPU on the Main Board. This interface consists of a Data Bus (DB7 - DB0), Address Bus (AB6 ~ AB1) Card Select (SL(2 - 0), ESA (2 - 0), IOSN), 2 Control Signals (LDSN, RWN) and 3 miscellaneous signals (SRSTN, IORDY, INTON, SCLK). Table 4 - 2 describes the CPU Port.

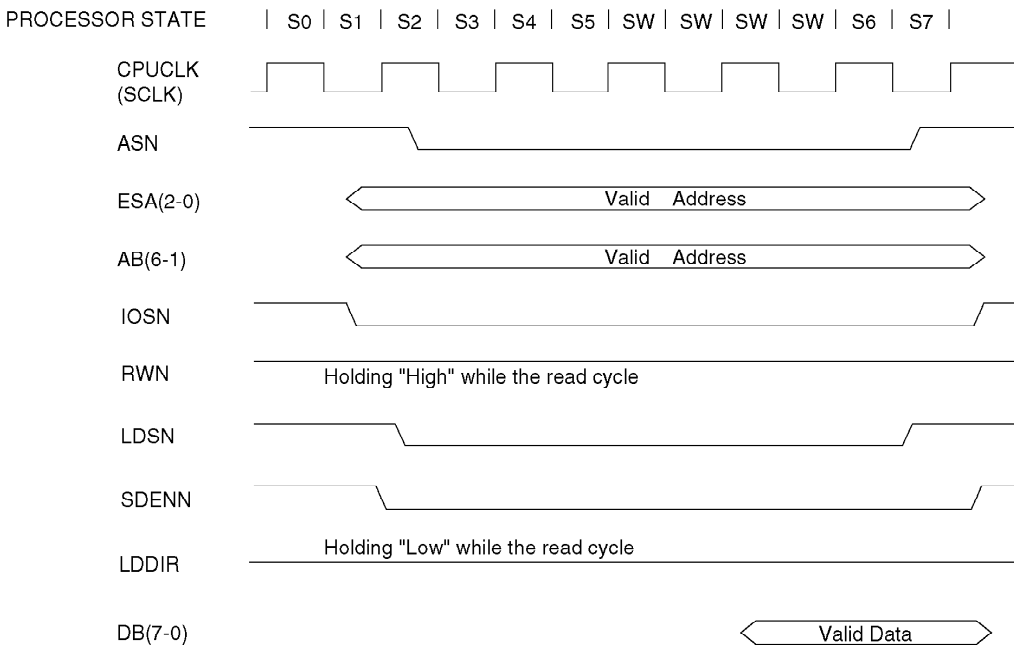
CPU Port of the Expansion Bus

Signal Name	Pin No.	Input/ Output	Explanation
DB (7 - 0)	10 ~ 3	I/O	8 bit bi-directional Data Bus. This data bus allows data transfer between I/O port in the add-in a CPU.
AB (06 - 01)	18 ~ 13	O	6 bit output Address Bus. These bits address the various registers in the add-in card. They select the internal registers in conjunction with card select control signals.
ESA (2 - 0)	23 ~ 21	O	3 bit expansion Slot Address Bus. These bits address one expansion Slot within other expansion s
SL (2 - 0)	36 ~ 34		3 bit expansion slot identity output. These bits are given to each expansion slot. It shows a unique slot number.
IOSN	24	O	Card Select output. This is an active low output, enabling the read or write operation various registers in the add-in card.
LDSN	27	O	Lower byte Strobe output. This output activates the Address Bus and RWN output and ena transfers on the Data Bus.
RWN	28	O	Read Write Control output. This output controls the direction of data flow on the data bus. When High, the I/O buffer acts as an output drive and as an inpu when low.
SRSTN	33	O	System Reset Output. This is an active low output, resetting all the registers in the add
INTON	30	I	Interrupt Request input. (Open Collector) This active low input notifies the controlling CPU of an interrupt
IORDY	29	I	IO Data Ready input. (3 state) This active High input indicates the current bus cycle is complet add-in card negates this signal at the current bus cycle, when th addresses the slower device on the add-in card, the current bus waits until IORDY asserts to High.
SCLK	37	O	System Clock output. This clock output is the same as SPUCLK (12.288MHz).



(3) DSP Card Read Cycle By CPU

DSP Card Read Cycle by CPU

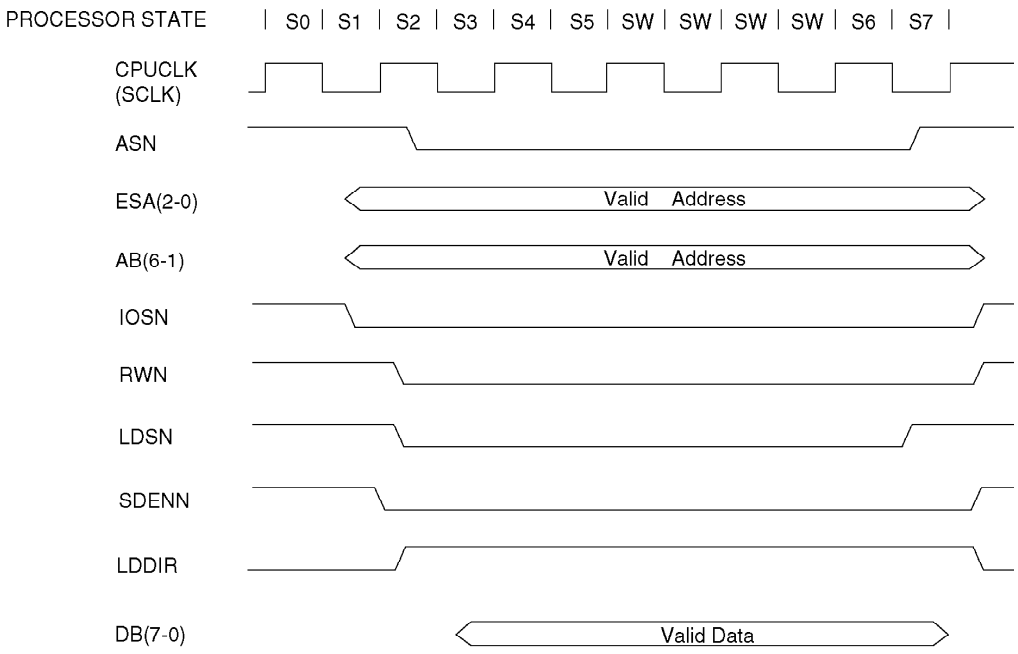


The CPU (IC301) outputs Valid Address to ESA (2 - 0) in S1 State. System Controller (IC302) asserts IOSN in low. CPU holds RWN High, asserts LDSN in low, in the period from the rising edge of S2 state to the falling edge of S6 state. DSP card outputs the register condition corresponding with AB (6 - 1) and ESA (2 - 0) to DB (7 - 0). CPU takes effective data on DB (7 - 0) in the falling edge of S6 state. In Read Cycle SDENN (pin 19), control signal of IC318 (LS245 - Bus Transceiver) is asserted by system controller in the period from S1 State to S7 State in low. LDDIR (1 pin) is asserted in low.

(4) DSP Card Read Write By CPU

CPU (IC301) outputs Valid Address to AB (6 - 1) and ESA (2 - 0) in S1 State. System Controller (IC302) asserts IOSN in low. CPU asserts RWN in S2 State in low, and outputs write data from S3 state onto DB (7 - 0). CPU asserts LDSN in lo w in the period from the rising edge of S2 state to the falling edge of S6 State. DSP card takes effective data on DB (7 - 0) in the rising edge of LDSN. In Write Cycle SDENN (pin 19), control signal of IC308 (LS245 - Bus Transceiver) is asserted by the system controller in the period from S1 State to S7 State in low.

DSP Card Write Cycle by CPU



(5) Overview of the Serial Voice Port

Voice Port lessens the connecting signal line between the CPU and DSP Card. This time-share serial bus is designed to realize transmitting sufficient data in its performance. The Control section on the host (CPU) side is the master controller and the control section on the DSP card side is the slave controller.

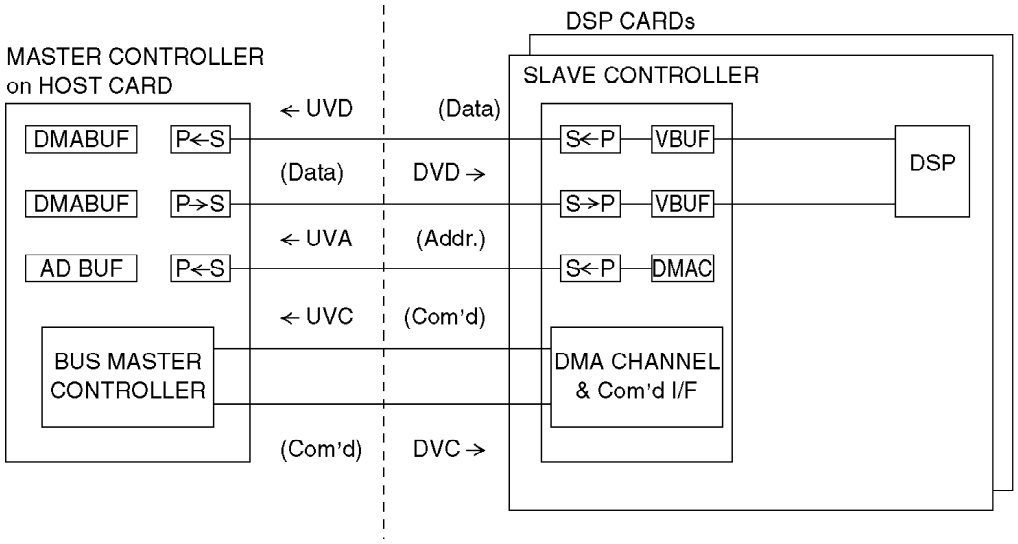
Data for two kinds of 32 channels passes through on this bus. Data types are ADPCM VOICE Data (32kbps/CH) and DPT Data (max 32kbps/CH). The Time slot passes through individual data called VOICE Channel and PT Channel.

Voice Channel

Voice Channel is a serial bus with bit rate : 2MHz and practice data transfer ability : 32 kbps, and each individual channel is in the 32 time- share. Normally ADPCM compressed voice data is passing through.

DMA data transfer method is offered by Voice Channel. The cooperation DMA channel inside the slave controller and bus masterlogic inside the master controller makes it possible for DMA data between the voice buffer inside the controller and host memory to transfer.

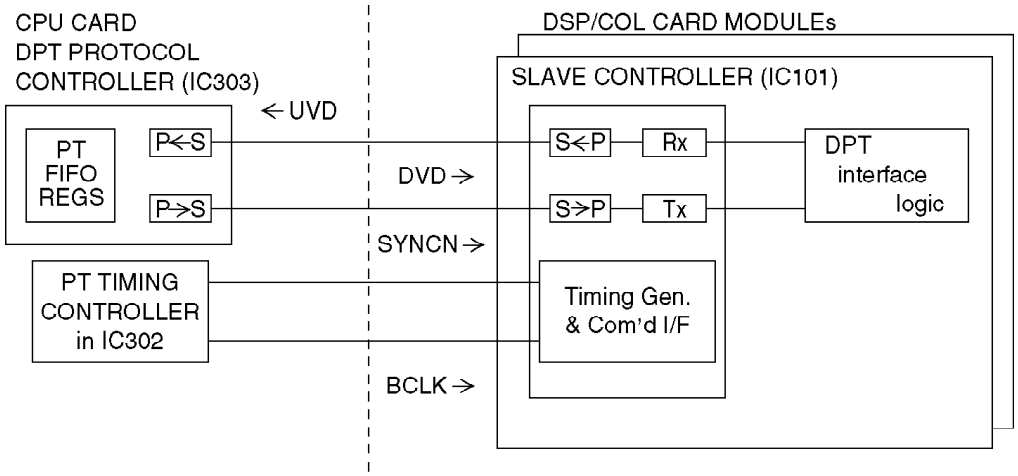
Voice Channel on the Voice Port



In DSP/CO Card Module, voice Band digital data is received from the circuit : T-R line is input by DSP, and DSP executes voice data's ADPCM compressing disposition. Compressed ADPCM data is stored in the voice buffer inside the slave controller by DSP. Voice Channel transfers DMA to host memory by the speed of 32kbps/channel.
In time recording disposition (voice compression) ADPCM data stored by DSP in the voice buffer inside the slave controller, data transfer and address information, and DMA channel inside the slave controller, are output to the voice channel. Based on this information, master controller drives inside its bus master logic, holding CPU, then stores ADPCM data input from Voice Channel on host memory.
In play-back disposition, ADPCM data on host memory is stored in the voice buffer inside the slave controller from the voice channel. ADPCM data inside the voice buffer is restored to voice band digital data by DSP, and sent out to the line : T-R line.
In this playback disposition, data transfer information and address information generated by the DMA channel inside the slave controller are output to the voice channel. Based on this information, master controller drives in its bus master logic, holding CPU, then transfers ADPCM Data from host memory to the Voice channel buffer inside master controller. The data stored in the Voice channel buffer is transferred to the VOICE channel buffer inside the master controller through the voice channel. DSP takes over ADPCM from this voice buffer.

PT channel
PT Channel is a time-share bus of 2Mbps and 16 bit × 32channels. It realizes transmitting data between DPT buffer inside the slave controller and HDLC controller on the Main Board. The data, sent and received in DPT buffer inside the slave controller through the PT channel, is sent and received by the PBX through interface logic.

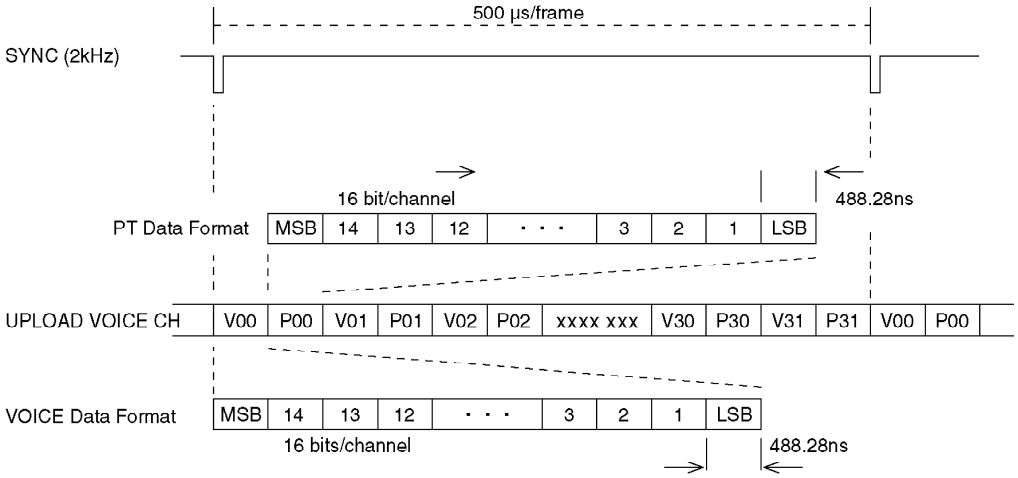
PT Channel on the Voice Port



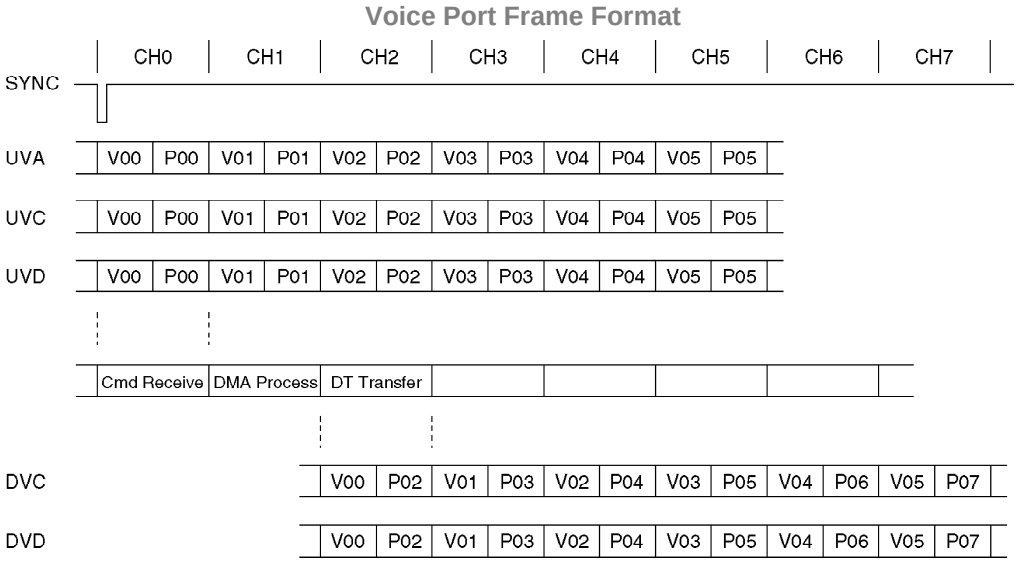
When receiving and sending DPT data, data transfer between the DPT protocol controller (IC303) on the host card and the PT buffer inside the slave controller (IC101) is realized. PT control logic inside the master controller (IC302) controls the receiving and transfer timing of the DPT protocol controller on the host card. The data channel component is extracted from the DPT data received from the circuit line by interface logic, then stored in the PT-RX buffer inside the slave controller. DPT data stored in the PT-RX buffer inside the slave controller is input in the DPT protocol controller on the host card through the PT channel. The PT-RX buffer size inside the slave controller is 8 bit.
DPT data to be sent out from the circuit line is stored in the PT-TX buffer inside the slave controller from the DPT protocol controller through the PT channel. DPT data stored in the PT-TX buffer is symbolized by interface logic and output from the circuit line. The PT-TX buffer size inside the slave controller is 8 bit.

(6) The Frame Format of the Voice Port
Voice Port is composed by five lines, SYNCN (Synchronization pulse) directs master controller slave controller (down road), BCLK (Bit Clock), DVD (Download-Voice-Data), DVA (Download-Voice Address) and DVC (Down load-Voice command), two signal lines, and UVD (Upload-Voice-Data) directs master controller (up load) and UVC (Upload-Voice-Command).
Master controller outputs frame pulse (SYNCN : 2kHz) and Base Clock (BCLK : 4.096MHz) to the slave controller for synchronization.
Voice Port is 500 μ s/32 channel time share bus, synchronized with SYNCN generated from the Master Controller. One frame of the voice port is 500 μ s and VOICE/PT DATA of 32 channels pass through time share. VOICE/PT DATA maximum 1x32 channel/frame can pass through one frame period. Each VOICE Channel/ PT channel is composed of 488ns/bit (2.048MHz) x 16bit (= 7812ns), the arrangement of each channel is from the head VOICE channel : 0, PT channel : 0, VOICE channel : 1, PT channel 1, ..., VOICE channel : 31, PT channel : 32.

Voice Port Timeslot Assignment


500 µs/frame
SYNC (2kHz)
16 bit/channel
488.28ns
PT Data Format
MSB 14 13 12 · · · 3 2 1 LSB
UPLOAD VOICE CH
V00 P00 V01 P01 V02 P02 xxxx xxx V30 P30 V31 P31 V00 P00
VOICE Data Format
MSB 14 13 12 · · · 3 2 1 LSB
16 bits/channel
488.28ns

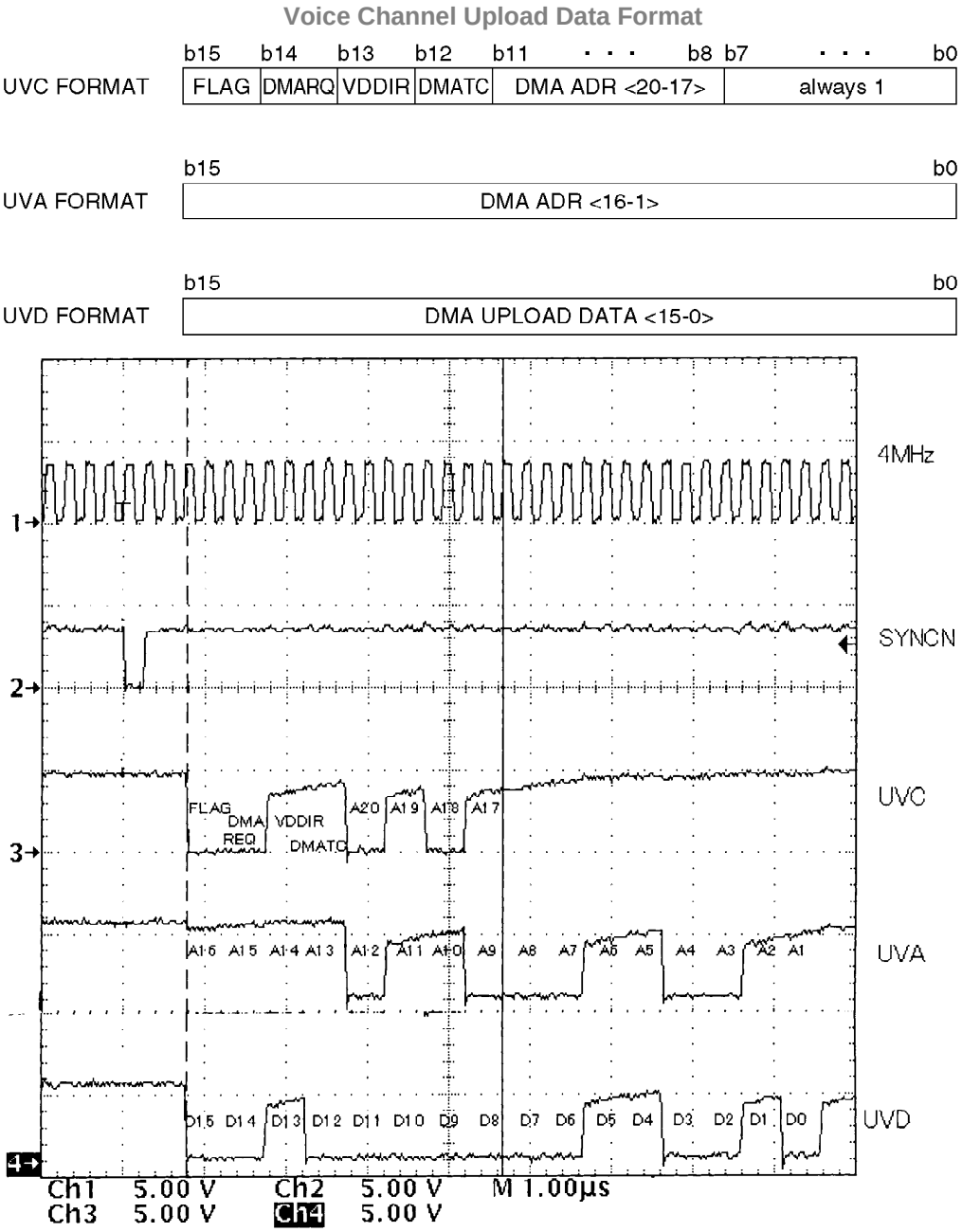
Host CPU programs the slave controller. The slave controller assigns the channel which can be used. Time slot logic inside the slave controller, corresponds with this channel assignment, decides the channel slot available for itself and make required control signals from the frame pulse and 4MHz clock.
In VOICE channel, down load timing is behind the time for 64 bit (31.24 µ s) in regard to up load timing. Voice channel offers a DMA transmitting method. For this reason, command reception of the master command and latency for direct memory access are added.
In case of down loading play back data from the host memory to the DSP card using DMA data transfer; eg, VOICE data, responded to DMA data transfer command up-loaded in CH0, is down loaded in the timing of CH2. VOICE channel defines each channel, up-loaded at the time SYNC is being asserted, as CH0, thereafter, CH1, CH2,...CH31.
PT channel has no DMA data transfer function. Referring to external-fixed HDLC controller and interface, up load channel and down load channel are the same timing.


Voice Port Frame Format
CH0 CH1 CH2 CH3 CH4 CH5 CH6 CH7
SYNC
UVA V00 P00 V01 P01 V02 P02 V03 P03 V04 P04 V05 P05
UVC V00 P00 V01 P01 V02 P02 V03 P03 V04 P04 V05 P05
UVD V00 P00 V01 P01 V02 P02 V03 P03 V04 P04 V05 P05
Cmd Receive
DMA Process
DT Transfer
DVC V00 P02 V01 P03 V02 P04 V03 P05 V04 P06 V05 P07
DVD V00 P02 V01 P03 V02 P04 V03 P05 V04 P06 V05 P07

(7) The Data Format of the Voice Port

VOICE CHANNEL Data Format

Format of the VOICE channel in up load channel is defined as follows.



FLAG bit of command channel is a signal that indicates the DMA channel inside the slave controller to start transmitting effective data and Low assert.
DMARQ bit is a DMA request signal, against the DMA channel inside the slave controller. It asserts when DSP on the DSP card requests host memory to transfer DMA data and it is in Low assert. The Master controller motivates the DMA data transfer process for the channel and its main bit is asserted.
DMATC bit is a TC (Transfer Complete) signal asserted when the number of times the DMA channel inside the slave controller executed, reaches the regulated number of times and low assert. This bit is asserted only once when it reaches TC, this bit is latched the inside master

controller and informed to the host CPU as a DMATC intrusion.
DMA ADR(20 - 1) bit, divided in the command and address channel, is an address on system memory existing as ADPCM data.
In case of down loading play back data from the host memory to the DSP card using DMA data transfer; eg, VOICE data, responded to DMA data transfer command up-loaded in CH0, is down loaded in the timing of CH2. VOICE channel defines each channel, up-loaded at the time SYNC is being asserted, as CH0, thereafter, CH1, CH2,...CH31.
DMA DATA (15 - 0) allotted to the data channel is up load data to be a DMA object. This data is ADPCM voice data to be stored in system memory, compressed on the DSP card.
The mode of DMA can be divided into two groups because of the direction of the DMA transfer. First, in the case of the DSP card' host memory; data is transferred from a 16 bit voice buffer inside the slave controller to a DMA data buffer inside the master controller. The Slave controller is asserted as DMARQ to command channel, DMA address is placed on the address channel, and data is placed on the data channel. Then these are transferred to the master controller. Master controller stores transferred command/address/data in a DMA buffer temporary, then requires the host CPU to hand over Bus Ownership. When host CPU releases, the bus master controller executes a transfer from DMA buffer to host memory.
Second, in the case of host memory ' I/O card, data is transferred from a 16 bit DMA data buffer inside the slave controller to a voice buffer inside the I/O card. Slave controller is asserted as DMARQ to the command channel, DMA address is placed on the address channel, then these are transferred to master controller. Master controller stores transferred command/address/data in a DMA buffer temporarily, then requires the host CPU to hand over Bus Owner ship. When host CPU releases, the bus master controller reads data from the host memory, in the next phase through up load bus transfers data to slave control.

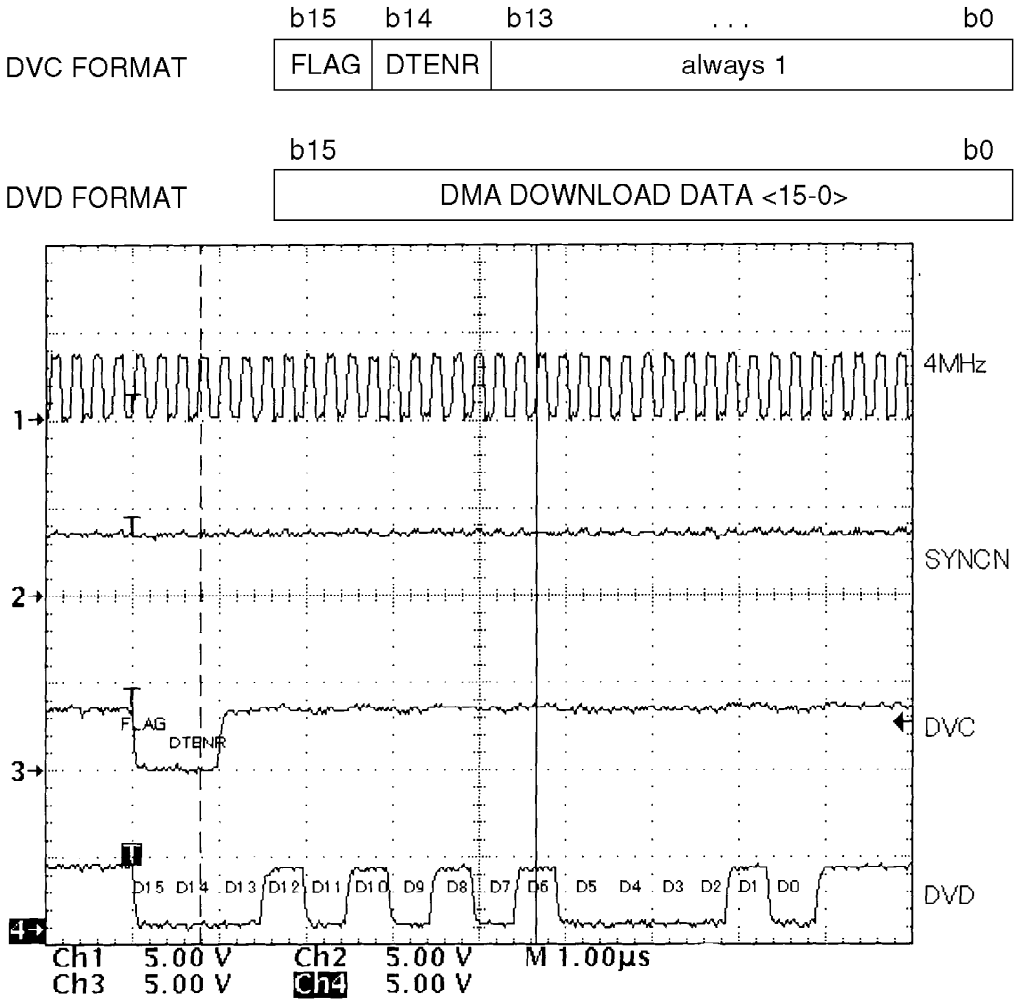
Mode phase of the VOICE channel by up load command is as follows.

[TYPE OF UPLOAD COMMAND]

DWAIT	DMARQ	VDDIR	DMATC	FUNCTION
0	0	0	1	HOST → I/O CARD DMA Request
0	0	1	1	I/O CARD → HOST DMA Request
0	0	0	0	HOST → I/O CARD DMA Request with TC flag
0	0	1	0	I/O CARD → HOST DMA Request with TC flag
1	x	x	x	idle State

Format of down load channel is defined as follows.

Voice Channel Download Data Format



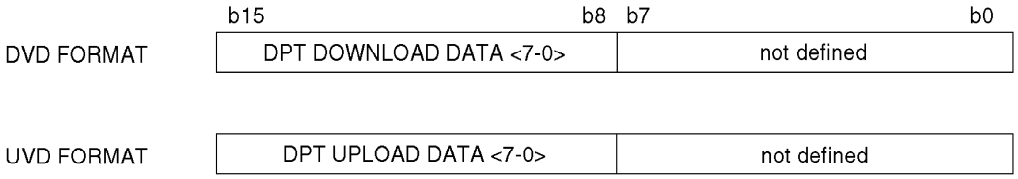
The Down load channel has only a command channel and data channel.
FLAG bit of the command channel is a signal indicating the master controller to start effective data transfer, and low assert.
The meaning of DTENB bit differs with the direction of data transfer.
In master controller' slave controller direction transfer; it is indicated that data on the data channel sent by the master controller is the same as the data on the host memory requested from the DSP card.
Slave controller' master controller direction controller, it is indicated that effective data sent from the slave controller is stored in system memory. This bit is low assert.
DMA transfer direction is host' DSP card; the effective data should be transferred from a 16 bit DMA data buffer inside the master controller to a voice buffer inside the slave controller. Master controller stores DMA address sent from the DMA channel inside the slave controller together with a DMA request in the DMA buffer temporarily, then requires host CPU to release bus. When host CPU releases, master controller reads data from host memory, then transfers effective data to the slave controller through the down load channel in the following phase.

Mode phase of the VOICE channel by up load command is as follows.

[TYPE OF UPLOAD COMMAND]

START	DMAEN	FUNCTION
0	0	Requested DMA Transfer Succeed
1	x	idle State

PT CHANNEL data Format
PT channel uses only data line and its format is defined as follows.

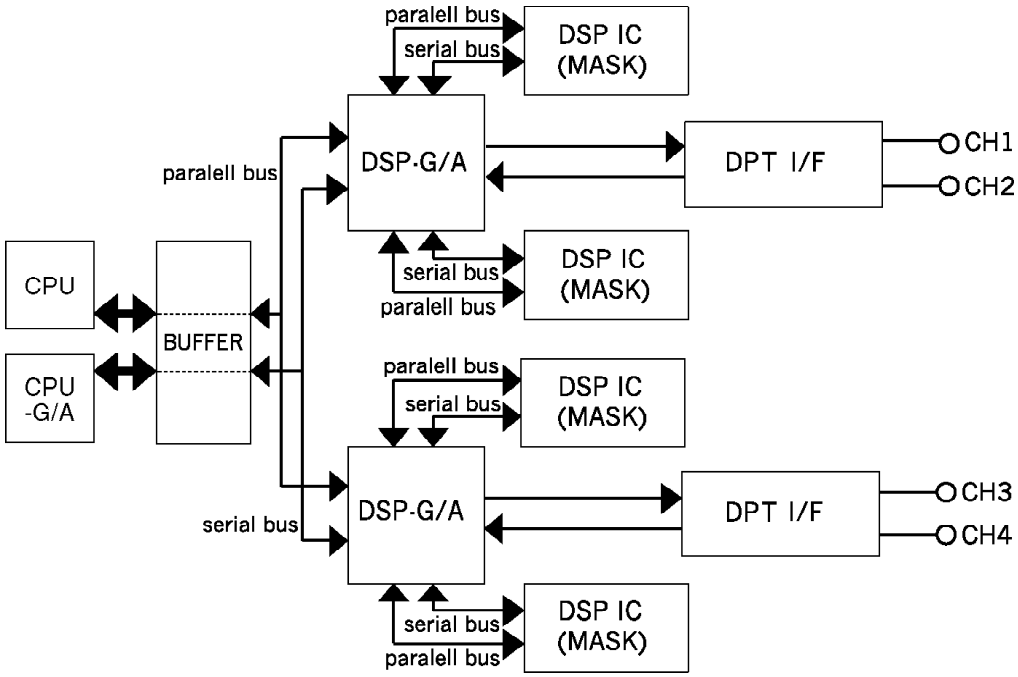


DATA (7 - 0) allotted to the down load channel indicates DPT DATA to be sent to the PBX, DATA (7 - 0) allotted to the up load channel indicates DPT data received from the PBX.

8.2. KX-TVS204

8.2.1. OVERVIEW

The KX-TVS204 (4DPT card) with 4 ports is optionally mounted on the KX-TVS300 for DPT interfacing only. It shares the same circuit board outline with the existing DSP card of the KX-TVS102. Along with the single circuit board design, DSP IC masking and the creation of six circuit board layers have been implemented. The general configuration is shown in the illustration below.



The KX-TVS204 has a construction in which the existing KX-TVS102 DPT interface sections are

connected through a dual buffer system. Two DSP gate arrays and four mask DSP ICs are mounted as a result. Two ports are provided, and by using only high/low lines, DPT communication for two channels is enabled using a single port, and communication for 4 channels is enabled using two ports. The host CPU must identify the previously mentioned slot addresses and card identification addresses for the KX-TVS204.

The function of the DSP Card is integrated in the Slave Controller (IC101) and DSP (IC109). These LSI devices include the functions mentioned below.

Slave Controller

- **FIFO to communicate between CPU and DSP.**
- **Voice Port Interface to transfer ADPCM data between system memory and DSP.**
- **DPT interface to receive and send digital data by DPT protocol.**
- **Line interface control I/O port to detect BELL, off-hook control, etc.**

DSP (IC109)

- **Compression/extension of voice data by ADPCM algorithm.**
- **To detect and generate DTMF.**
- **To detect and generate TONE.**
- **Detection of VOX (no-sound) condition. (To detect the condition of completed conversation.)**
- **Automatic gain adjustment of recording level.**

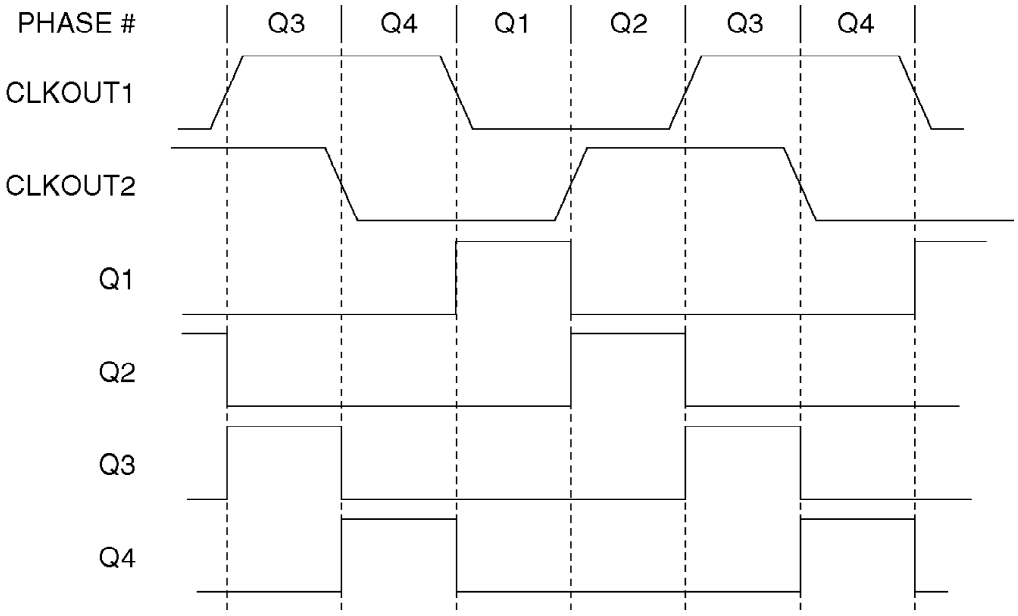
8.2.2. CPU BOARD INTERFACE

Refer to EXTENSION BUS (DSP CARD INTERFACE).

8.2.3. DSP CLOCK

4.096MHz provided from the CPU board is input to the DSP (IC109(pin53)) as a basic clock. This clock is input to the PLL inside DSP. PLL generates 14.336MHz(PLLCLK) from this clock. PLLCLK is divided into four inside and generates CLKOUT1 and CLKOUT2.
Figure 4 - 22 is standing of CLKOUT1 and indicates the third phase (Q3) is about to begin. Hereafter, phase no. Q1 - Q4 explains the bus operation.

DSP Clock



8.2.4. PARALLEL DSP PORT

DSP installs control signals mentioned below to interface with Program ROM or a IC101 inside register.

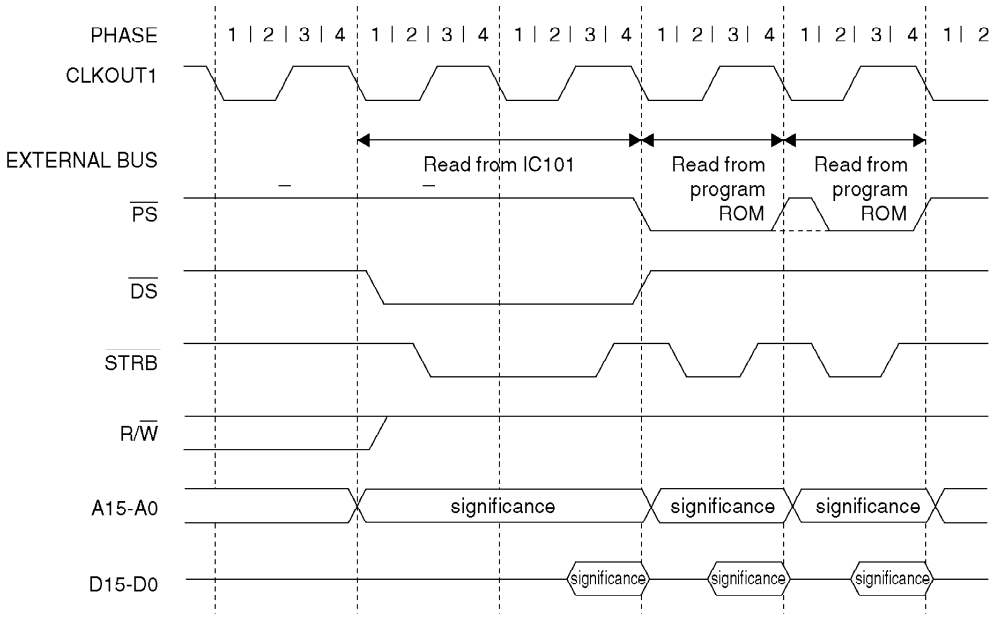
- **16bit parallel data bus (A15 - A0)**
- **16bit parallel data bus (D15 - D0)**
- **Chip select (PS, DS)**
- **Timing Control (STRB, R/WN)**

(1) External read out cycle
The following are phenomena generated with the external read out cycle.

1. **In the first phase (Q1), DSP starts driving address bus, and makes either PS or DS low level. To indicate the external memory's read out, R/W signal becomes high level.**
2. **At the beginning of the second phase (Q2), STRB signals indicating the effectiveness of the address bus output, and is used to generate a read enable signal with the R/W signal.**
3. **At the end of the third phase (Q3), data is taken in.**
4. **At the beginning of the fourth phase (Q4), the STRB signal is cancelled. PS, or DS signal and address bus are of no effect, and ends the external read out cycle.**
   Control signal PS, DS, STRB and R/W are generated only when the external memory location has gained access to. PS is

asserted only when Program ROM (IC107/IC108) has gained access. DS is asserted only when the internal register of IC101 has gained access.

Read Cycle

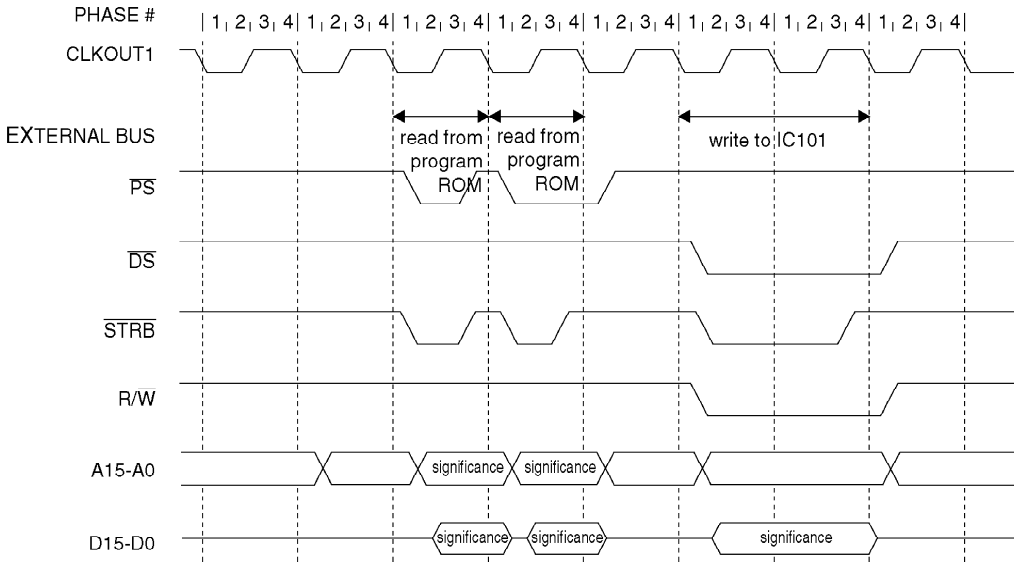


(2) External write in cycle

The following are phenomena generated with the external write in cycle.

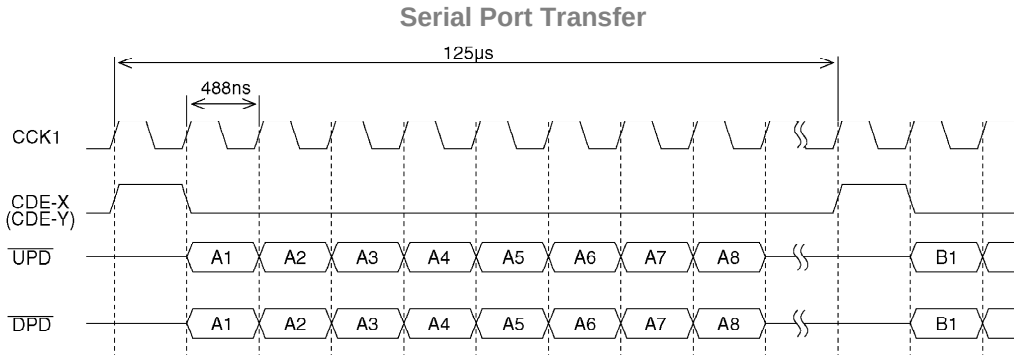
1. **In the first phase (Q1), DSP starts driving address bus, and makes DS active low. The R/W signal be comes low level for writing in external memory.**
2. **At the beginning of the second phase (Q2), the STRB signal indicates the effectiveness of the address bus output, and is used to generate read a enable signal with the R/W signal.**
3. **At the beginning of the second phase (Q3), data bus becomes active.**
4. **At the beginning of the fourth phase (Q4), the STRB signal is canceled. The Processor makes the address bus and DS signal invalid, and ends access of the external write in cycle.**

Write Cycle



8.2.5. DSP SERIAL PORT

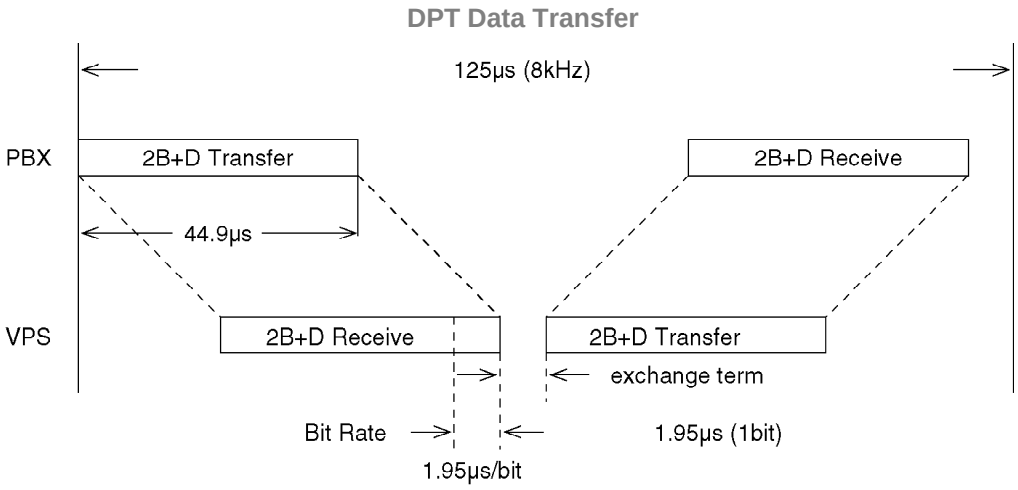
DSP serial port is used with the interface for the DPT B channel (Digital Voice Data).
This port is connects IC101 with CCK1, UPD, DPD, CDE-X(IC109A) and CDE-Y(IC109B) signals. CCK1 is a 2.048MHz's serial shift in/out clock. UPD is 8bit PCM formatted voice data output from DSP. It is sent out to the PBX through DPT interface logic internal IC101. DPD is DSP input of PCM formatted voice data received from the PBX. CDE-X(CDE-Y) is an 8kHz frame pulse input to enable to send or receive effective data of a serial port.



8.2.6. DPT DIGTAL INTERFACE

DPT digital interface is provided with IC101. DPT interface built-in IC101 extracts effective data (2B + D) from a receiving DPT data stream, transfers D channel receiving data to voice port, and B channel receiving data (PCM Voice Data) to DSP. Sending out DPT data stream formed with D channel sending out data received from Voice Port and B channel sending out data received from DSP, is output to the COL card.
DPT interface is a digital interface, line bit rate : 512kbps's, 2 line time share data format. Its communication format is 2B+D (B:64kbps, D:16kbps) and executes ping-pong communication every 8kHz (125 µ s).

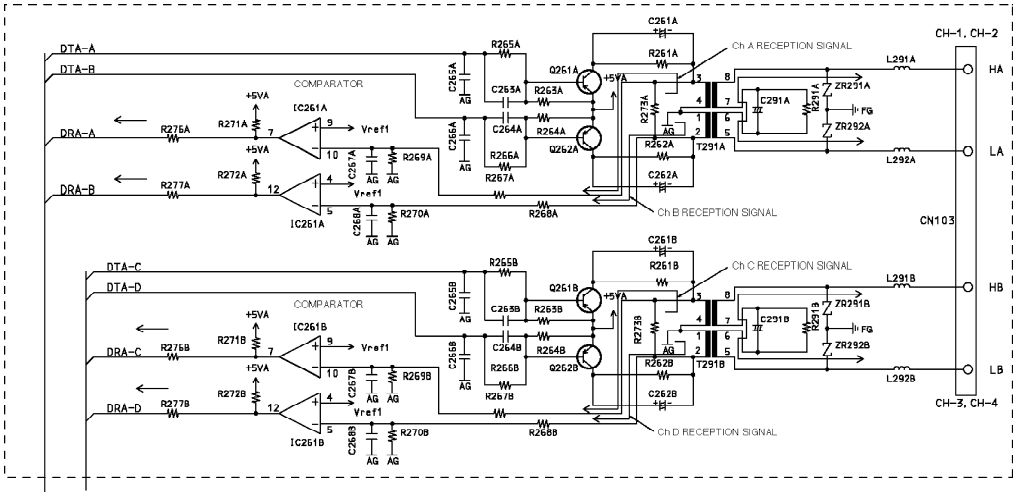
Data format B channel is 64kbps µ /A PCM format and D channel is 16kbps HDLC format.



Bit allotment of the DPT frame is described below. S(1 - 5) is a zero pattern of 5 bits and is used as hardware to synchronize receiving and sending data with PLL.MA (1 - 3) is a 3-bit zero pattern data against AM1 symbolization and is used to detect the head of effective data. HK sends out an installed value inside the HK port. D(0 - 1) is 2 bit/frame HDLC data channel. B1 (7 - 0), B2 (7 - 0) are received and sent out in an 8-bit PCM data by MSB first individually.

S	S	S	S	S	M	M	M	H	D	D	B	B	B	B	B	B	B	B	B	B	B	B	B	B	P
1	2	3	4	5	A	A	A	K	0	1	1	1	1	1	1	1	1	2	2	2	2	2	2	2	R
					1	2	3				7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	Y
5					3			2			8								8							1	

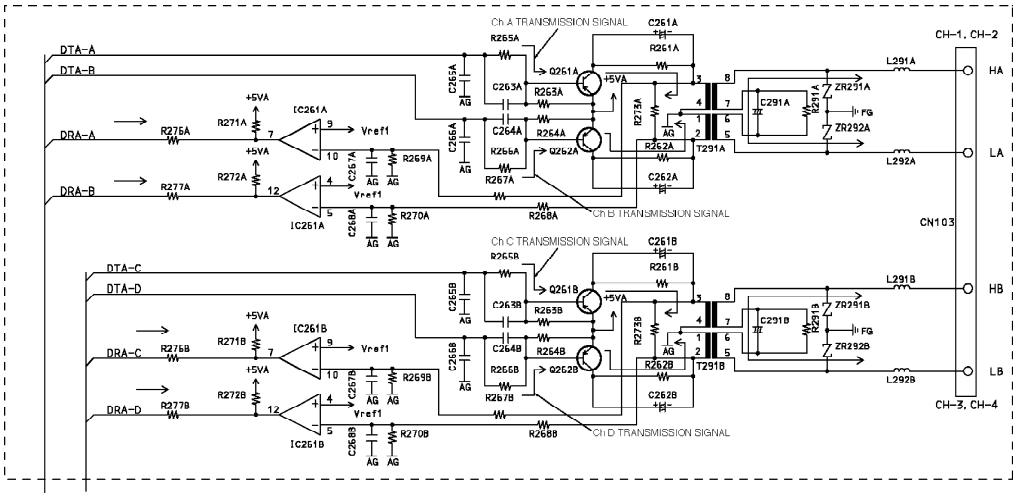
8.2.7. DPT LINE RECEIVER



This logic allows the DPT to receive reception data from the PBX.
The DPT reception data flows through HA → L291A → T291A (pin8 - pin7) → C291A → R291A → T291A (pin6 - pin5) → L292 → LA

HB → L291B → T291B(pin8 - pin7) → C291B → T291A(pin6 - pin5) → L292B → LB

8.2.8. DPT LINE TRANSCEIVER



This logic allows the DPT to transmit transmission data to the PBX.
The DPT transmission signals flow as follows.

DTX - A = IC101A(pin17) → R113A → R265A → Base of Q261A.
DTX - B = IC101A(pin18) → R114A → R266A → Base of Q262A.

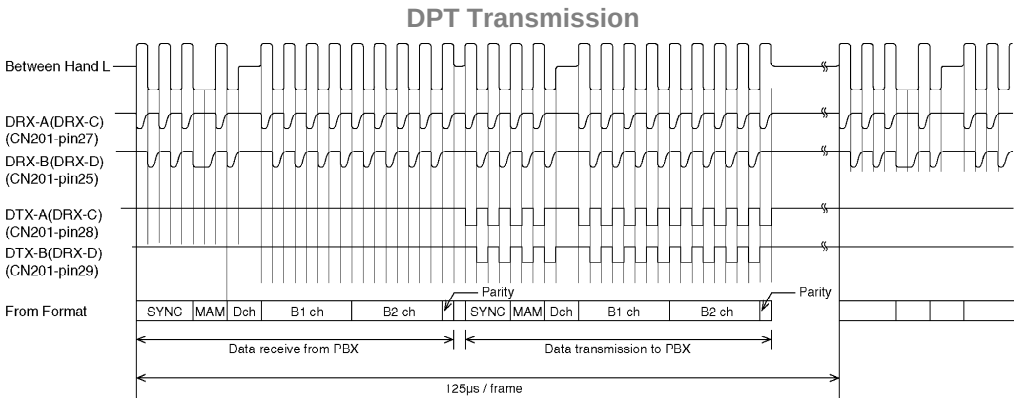
DTX - C = IC101C(pin17) → R113B → R265B → Base of Q261B.
DTX - D = IC101B(pin18) → R114B → R266B → Base of Q262B.

If IC101A drives DTX - A (DTX - B) to low level, Q261A (Q262A) is turned ON and the loop current flows through
If IC101B drives DTX - C (DTX - D) to low level, Q261B (Q262B) is turned ON and the loop current flows through as follows.

+5VA → Q261A (pinE - pinC) → C261A → T291A (pin3 - pin4) → AG
+5VA → Q262A (pinE - pinC) → C262A → T291A (pin2 - pin1) → AG

+5VA → Q261B (pinE - pinC) → C261B → T291B(pin3 - pin4) → AG
+5VA → Q262B (pinE - pinC) → C262B → T291B(pin2 - pin1) → AG

This loop current transition generates the DPT transmission data between T291A/T291B - pin 8 and T291A/T291B(pin 5).
As a result, T291A/T291B drives the HA/HB - LA/LB line corresponding with DTX-A/DTX-B.



8.3. POWER SUPPLY BOARD

8.3.1. OUTLINE

Outline of power supply board

The power supply board on the KX-TVS120 is a 120V-input, separately excited switching power supply. There are four secondary outputs: 12V for driving the hard disk drive motor, 5V(B/U) with and 5V without instantaneous power failure backup for driving the logic system, and -5V for driving the interfaces.

The unit's protection functions include the DC alarm detection function, overvoltage detection function, and overcurrent detection function.

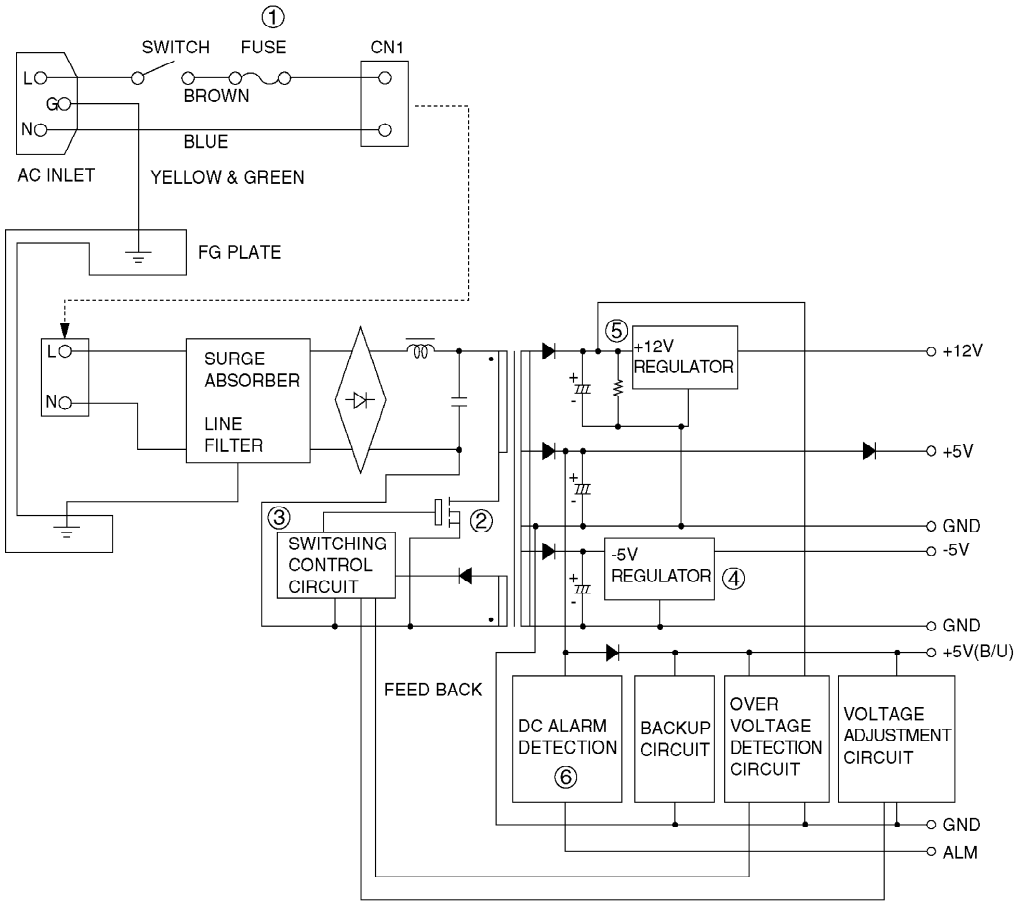
Surge absorbers are provided between the lines and between the unit and ground at the primary side of the power supply circuit, and the immunity from surges is further improved by incorporating a gap type of absorber between the unit and ground. A Line-filter, which is designed to improve the harmonic characteristics and which complies with the IEC950 standard, is provided at the primary side. The electrolytic capacitor for primary side smoothing has a large capacity to provide back-up during instantaneous power failures, and it comes with a cover to prevent a fire from spreading in the event of trouble. A FET is used for primary side switching, and an AC/DC converter control IC is employed for its control section. This IC provides the overcurrent detection function, overvoltage detection function, and soft start function.

The secondary side circuitry of the power supply consists of three systems which deliver +12V, +5V and -5V through the power transformer. The +5V system is further divided into a +5V(B/U) circuit with a backup function and a +5V circuit without a backup function. The +12V and -5V voltages are generated by using a 3-pin regulator to drop the rectified DC voltages supplied from the transformer. The overvoltage detection circuit monitors the +12V and +5V(B/U) voltages of the secondary side circuit. The overcurrent detection circuit serves to narrow down the originating output when an overcurrent occurs in one of the secondary side systems. The +5V(B/U) system with the backup function supplies power to the logic system circuit; the +5V system without the backup function supplies power Remote Modem Card, to the LED and RS-232C driver. The +5V(B/U) system with the backup function uses a 4.7F × 3 super capacitor to back up the logic system circuit when an instantaneous power failure occurs. It also takes action in an instantaneous power failure: as soon as the supply of power from the primary side to the secondary side is interrupted in response to the monitoring of the DC alarm detection circuit, a DC alarm signal is output from the power supply and input to the CPU port.

A block diagram of the unit and a description of its operation are presented below.

Note:
Replace a whole power supply board without replacing individual parts on board.

8.3.2. BLOCK DIAGRAM

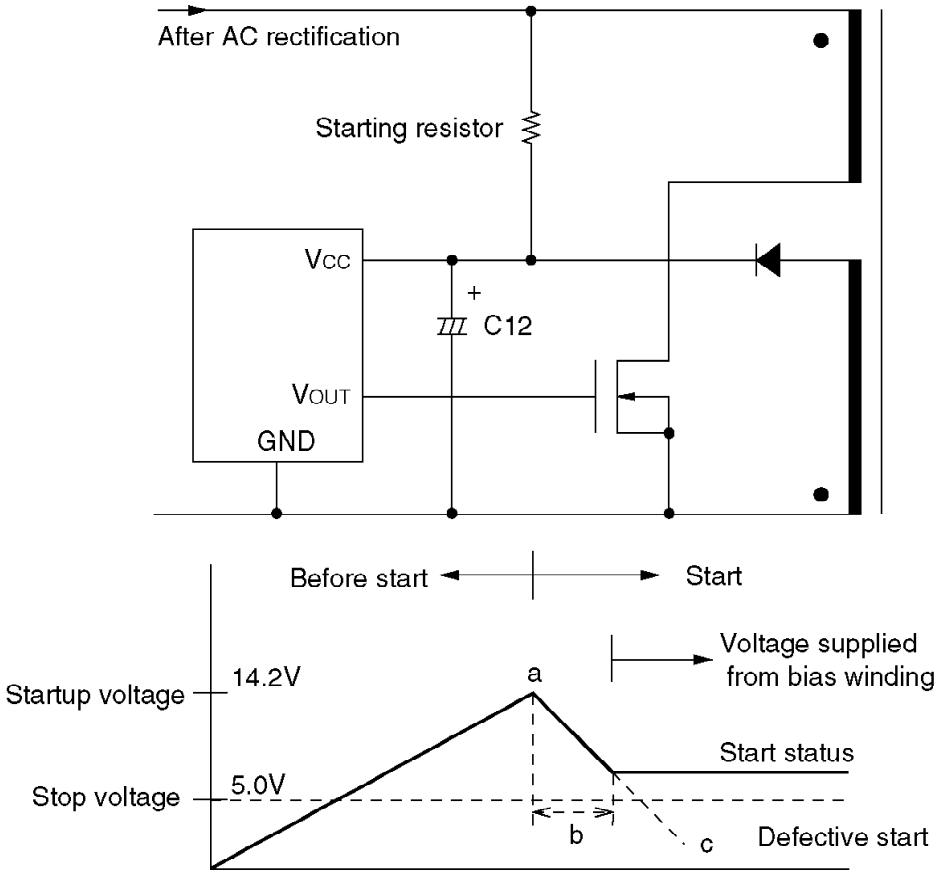


Schematic diagram ..... Refer to POWER SUPPLY BOARD.

8.3.3. CIRCUIT OPERATION

Start/stop circuit section (start mechanism)
After the AC voltage is supplied to the section, the supply voltage has reached the startup voltage with the current from the starting resistor and the IC has started operating, the power MOSFET starts to be driven. This generates bias in the transformer, and the supply voltage is applied to the IC from the bias winding (point "a" in Fig. 1).
After the supply voltage has reached the startup voltage, a voltage is generated in the bias winding, and while an adequate supply voltage is supplied to the IC, the supply voltage of the IC is supplied by the capacitor (C12) which is connected to Vcc.
During this period (area "b" in Fig. 1), the supply voltage continues to drop, and if it drops below the stop voltage of the IC before an adequate supply voltage is supplied from the bias winding, the power cannot be started (status "c" in Fig. 1).

Fig. 1



Triangular wave oscillation:

Triangular waveforms are generated by a process of constant-current charging and constant-current discharging in the externally mounted capacitor which is connected to CT. The charging current to discharging current ratio is set internally, and the current value is determined by the externally mounted resistor which is connected to the RT pin.

The RT pin voltage is determined at the level where the internal reference voltage (determined by the zener diode and npn transistor VEB, and temperature-compensated) has been divided by means of a resistor, and thus it is minimally affected by temperature variations or fluctuations.

Over Voltage protection circuit

The power output has a self-diagnosis function which shuts down the power in order to protect the load in the event that a voltage which is abnormally higher than the normal output voltage is generated due to a failure in the control system, application of an abnormal voltage from an external source, or some other reason.(See Fig.2)

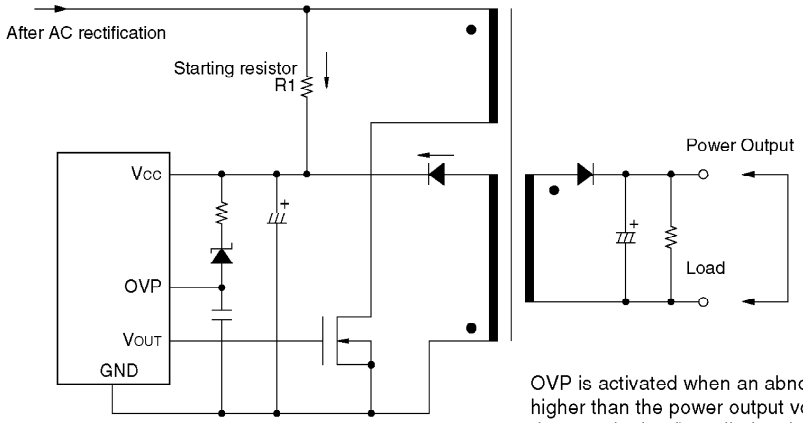
Basically, this function is set in such a way that the voltage at the Vcc supply voltage pin of the IC is monitored.

However, since the Vcc voltage is normally supplied from the transformer drive winding and it is proportionate to the secondary side output voltage, the function is also activated when a secondary side output overvoltage occurs.

1. **If the voltage which is input to the OVP pin has exceeded the threshold voltage (6.0V typ.) as a result of a power output abnormality, the internal reference voltage of the IC is shut down, all control is suspended, and this stop status is maintained.**
2. **OVP is released (reset) under the following condition:**

    - The supply voltage must drop (Vcc < 8.4V typ.: OVP release supply voltage).

If supply voltage Vcc during OVP operation is stable at a value higher than the OVP release supply voltage (which depends on the starting resistor), OVP will not be reset unless the AC input is cut off. (See Fig. 3)



OVP is activated when an abnormal voltage (which is higher than the power output voltage and which may damage the load) applied to the power output from an external source is detected by the primary side bias winding.

Fig. 2

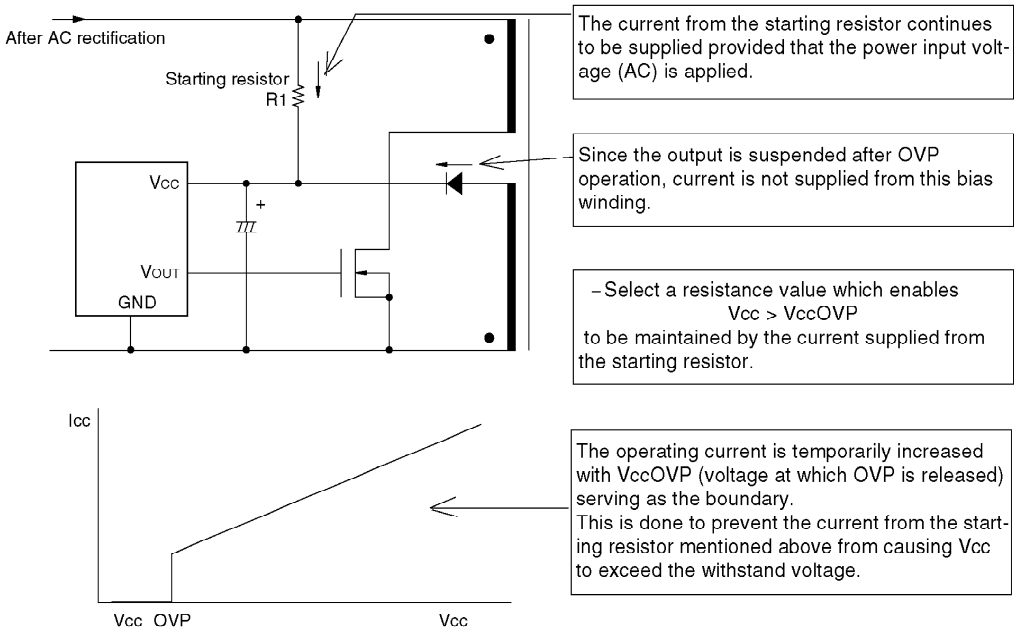

After AC rectification
Starting resistor
R1
Vcc
VOUT
GND
Icc
Vcc OVP
Vcc
The current from the starting resistor continues to be supplied provided that the power input voltage (AC) is applied.
Since the output is suspended after OVP operation, current is not supplied from this bias winding.
– Select a resistance value which enables Vcc > VccOVP to be maintained by the current supplied from the starting resistor.
The operating current is temporarily increased with VccOVP (voltage at which OVP is released) serving as the boundary.
This is done to prevent the current from the starting resistor mentioned above from causing Vcc to exceed the withstand voltage.

Fig. 3

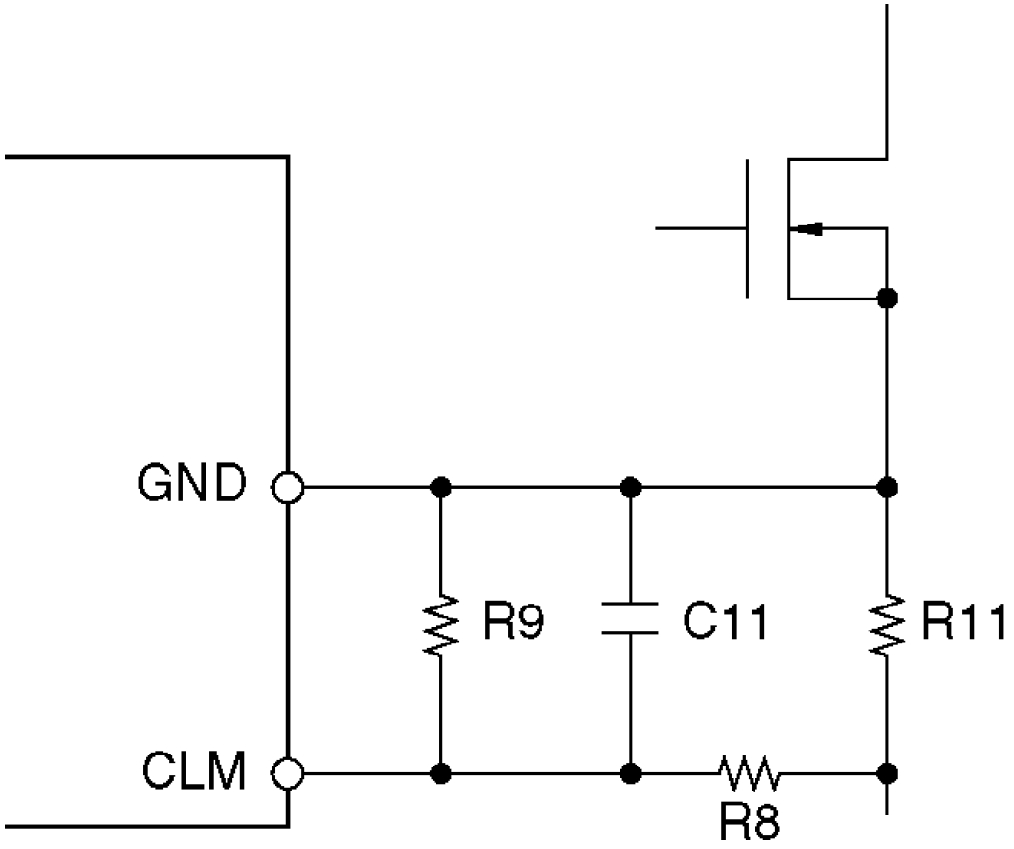
Overcurrent protection circuit

By utilizing the fact that overcurrent in the power output are proportionate to the current flowing to the primary side main switch (power MOSFET), the pulse current flowing to the main switch is provided with a ceiling. In this manner, this circuit limits these overcurrent in the power output and protects the components susceptible to overcurrent.

The current flowing to the main switch is detected by connecting a low resistance between the power MOSFET source and power supply GND and monitoring the voltage at both ends of the resistor. Control is exercised in such a way that, when the power MOSFET is turned on and the threshold voltage of CLM (current limit) is detected, the output is turned off, the power MOSFET is turned off, thus preventing a current exceeding this limit from flowing. The threshold voltage of CLM is approximately -200 mV (typ.) at an ambient temperature of 25°C in respect of GND of the IC. This control is repeated every cycle, and once an overcurrent is detected, the power MOSFET is kept in the OFF status for the rest of the cycle concerned, and it is not set on until the next cycle.

R8, R9 and C11 shown in Fig. 4 configure a filter circuit for filtering out the noise which is generated by the parasitic capacitance which is incidental in equivalent terms when the power MOSFET is turned on.

Fig. 4



DC alarm operation

During normal operation, zener diode D401 is turned on (it turns on at 4.2V or above), Q401 is ON and, as a result, a high signal equivalent to the +5V power supply is output to the CPU port as the DC alarm signal. When the power from the primary side of the power supply is no longer supplied, the voltage at both ends of D401 interrupts the 4.2V voltage, and first D401 is set off. As a result of this, Q401 is set off, a low signal close to ground potential is output to the CPU port and the CPU proceeds with the action which it takes when an instantaneous power failure has occurred.

Overvoltage detection circuit

The overvoltage detection circuit monitors the +12V and +5V voltages. In the case of the +12V voltage, the voltage before it is regulated to 12V is monitored, and when this voltage value exceeds 33V, D404 turns on, and the voltage is fed back to the primary side control IC via photo coupler PC2. Since the maximum input voltage of the +12V regulator IC is 35V, overvoltage detection is set to be activated at 33V, which is well within the 35V limit. In the case of the +5V

voltage, when the output voltage or the voltage applied from an external source exceeds 6.2V, D405 turns on, and the voltage is fed back to the primary side control IC via photo coupler PC2.

Voltage adjustment and feedback circuit
Shunt regulator IC103 is used for voltage adjustment and feedback. When the Vref voltage of IC103 is varied by varying VR101, the cathode voltage of the regulator is varied in proportion to the Vref voltage so that the current of photo coupler PC1 is controlled. As a result, the voltage of the +5V system can be adjusted. After the voltage has been adjusted, the shunt regulator operates in the same way as mentioned above in accordance with the voltage fluctuations in the +5V system to feed back a voltage which corresponds to the variation via the photo coupler to the primary side.

9. UTILITY COMMANDS

In this chapter, we explain commands which can be used by a general user.
In order to use, choose <Utility Command> in <System Administration Top Menu> of Administrator Service.
Command waiting prompt is on the screen. (See below.)
(Type "Kme" and enter password "Panasonic" to use all commands.)

```
$
```

Input command after "$".

```
$command
```

(Type "Kme" and enter password "Panasonic" to use all commands.)

9.1. HELP COMMAND (HELP)

1. FUNCTION
To show the list which can be used in the VPS.

2. OPERAND
Nothing.

3. HOW TO USE, EXAMPLE FOR USAGE

```
$HELP
      OFLN              :  System Off-line
      ONLN              :  System On-line
      PASS              :  Password setting
      TIME              :  Time & Date setting
      PSET              :  Report Print Out Time setting
      ELOG              :  Device Error Log Listing
      SAVE              :  VPS Program & Data Save (VPS -> PC : Xmodem)
      LOAD              :  VPS Program & Data Load (VPS <- PC : Xmodem)
      GPRN              :  Parameter Global Printing (only 'ASCII Terminal' mode)
      VERS              :  Program Version Check
      CREP [no]         :  Custom Menu Information List
                           [no]   :  Custom Menu No. (1-100)
      CCLR [no]         :  Custom Menu Access Counter Clear
                           [no]   :  Custom Menu No. (1-100/0) (0:Clear All)
      MWL               :  MWL Retry count Set (1-3)
      MRL               :  Minimum Recording Length Set (0-3)
      MPLT [opt]        :  Registered User Prompt No. List
                           [opt]  :  1       -->  User Prompt 1
                                     2       -->  User Prompt 2
                                     None    -->  User Prompt 1&2

- MORE -
      QSET              :  Quick Setup
      LMON              :  Line Monitor
      PUTD              :  DTMF Information Display (Don' t leave enabled after troubleshooting)
      WCID              :  Wait Time for Caller ID

- MORE -
      DCLR [drv], [opt] :  Initialize Parameters and Data
                           [drv]  1 or 2
                           [opt]  0 :  All Parameters and Voice Data
                                  3 :  All Parameters and Voice Data
                                                 except User Prompts
                                  4 :  All Voice DATA except User Prompts
                                  5 :  User Prompt-1 and User Prompt-2
                                  6 :  Only User Prompt-1
                                  7 :  Only User Prompt-2
      DCPY              :  Disk           Copy DISK1  =>  DISK2
      PCPY              :  Program        Copy DISK1  =>  DISK2
      GCPY              :  Guidance       Copy DISK1  =>  DISK2
      XCPY ([opt])      :  Program, System Guidance Copy DISK2   =>  DISK1
                           [opt]  None  :  Program and System guidance
                                  1     :  Program
                                  2     :  System Guidance
                                  3     :  User Prompts
      SYSD              :  System Disk Set Up (DISK2)
```

9.2. OFLN COMMAND

1. FUNCTION
To break VPS service.
VPS service is suspended.

2. OPERAND
Nothing.

3. HOW TO USE, EXAMPLE FOR USAGE
a) When throwing command, VPS service is not used.

```
$OFLN
** OFF LINE MODE **
```

- Becomes off line service immediately.

b) When throwing command, VPS service is used.

```
$OFLN
 *** Now Line is used !! *** < WAIT >
```

- The execution of this command is in the waiting condition, when service usage finishes, the command is executed.

```
** OFF LINE MODE **
```

9.3. ONLN COMMAND (ON LINE SERVICE CONTROL)

1. FUNCTION

VPS service is resumed.

2. OPERAND

Nothing.

3. HOW TO USE, EXAMPLE FOR USAGE

a) When throwing normal on line command

```
$ONLN
** ON LINE MODE **
```

b) Below mentioned cases don't become on line condition.

- In the DPT interface, DPT communication circuit is not connected. Or Communication circuit connected the install on PBX side is not shared as VM port in DPT interface.

- There is no DSP/CO card.

```
$ONLN
** OFF LINE MODE **
```

9.4. PASS COMMAND (SETTING PASSWORD)

1. FUNCTION

To set administrator and system passwords.

An Administrator password is the password to enter from the initial screen to the terminal select screen.

A System reset/clear password is the password to be asked when reset is executing on the <System Reset/Clear> screen.
Without a password, installation is possible in both cases.
The Password should be one word with less equal 10 letters or numbers, or special symbols (underline, period, space).

2. OPERAND
Nothing.

3. HOW TO USE, EXAMPLE FOR USAGE

```
$PASS
1 : Administrator Password 2 : System Reset/Clear Password : =
```

(1) IN THE OF CASE NEW REGISTRATION
Select 1 or 2.

```
$NEW PASSWORD : =
```

Input password.

```
$VERIFICATION : =
```

To confirm password, input password again.
When it is different from the first one, start from <New Password> again.
Note: Input password is not shown on the screen.

(2) CHANGE
Select 1 or 2.

```
$OLD PASSWORD : =
```

Input present registered password.

```
$NEW PASSWORD : =
```

Input new password.

```
$VERIFICATION : =
```

To confirm input password, input the password again.

Note:
When it is an administrator password, <present password> is not required.

(3) PASSWORD CANCELLATION
Select 1 or 2.

```
$OLD PASSWORD : =
```

Input present registered password.

```
$NEW PASSWORD : =
```

Press return key without inputting anything.

```
$VERIFICATION : =
```

Press return key without inputting anything.

9.5. TIME COMMAND (SETTING TIME/DATE)

1. FUNCTION
To set time and date.

2. OPERAND
Nothing.

3. HOW TO USE, EXAMPLE FOR USAGE

```
$TIME
Current time is 12 : 34, PM
Enter new time ( hh : mm, AM/PM ) : =
```

Input current time.
Example: In the case of 2:56 PM.
Enter new time (hh:mm, AM/PM) : = 2:56, PM

```
Current date is JAN-1-2001
Enter new date ( MM-DD-YY ) : =
```

Input current date (Month - Date - Year) (Input last two figures for year)

example: In the case of July 13th. 2001
Enter new date (MM - DD - YY) : = 7-13-01

Note:
Input time and date correctly, because VPS service owes much of its work to time and date. Following are also changed with the change of time and date. Notification of arrival, Message auto distribution send, Designated time between mail boxes message distribution send, Auto transfer function, etc.

9.6. PSET COMMAND (SETTING REPORT PRINTING OUT TIME)

1. FUNCTION
This command makes it possible to print out reports at a certain time. The Following reports are printed out.
(1) Disk Usage Report
(2) Port Usage Report
(3) Call Account data Report

2. OPERAND
Nothing.

3. HOW TO USE, EXAMPLE FOR USAGE

```
$PSET
Report Print Out Service [ Disable ]
1 : Enable 2 : Disable : =
```

Input 1 for install, input 2 for cancellation.
When you input 1, still more set the time for printing out.

```
Enter The Print Out Time ( hh : mm, AM/PM ) : =
```

Example: In the case of 2:56 PM Enter the Print Out Time (hh:mm, AM/PM) : = 2:56, PM

9.7. ELOG COMMAND (DISPLAY DEVICE ERROR)

1. FUNCTION
To display the error trace of the DSP card, MAIN board, Hard disk, etc.

2. OPERAND
Nothing.

3. HOW TO USE, EXAMPLE FOR USAGE

```
$ELOG
        DEVICE          ERROR               TIME
        - - - - -       - - - - -           - - - - -
1.      CPU             MEM-GET             JUL-14 14:00 PM
2.      CLOCK                               JUL-15 12:40 AM
3.      DISK            DATA R/W (xx/yyyy)  JUL-15 13:02 PM
4.      DSP1            SCAN                JUL-15 13:02 PM
5.      DSP4            FIFO                JUL-15 13:15 PM
6.      CPU             APPLICATION (2)     JUL-15 13:16 PM
```

[Explanation]

- The following examples of errors.

CPU	**MEM - GET**	**Main Board impossible to acquire memory.**
	APPLICATION (n)	**Application error occurred momentarily while working.**
CLOCK		**Hindrance occurred in clock IC.**
DISK	**DATA R/W (XX: YYYY)**	**R/W error in hard disk. (master)**
		XX : error code
		YY : error sector No.
DSPn	**SCAN**	**DSP Card n is not equipped.**
		CPU cannot confirm the DSP card.
	FIFO	**DSP or FIFO error occurred momentarily while working.**

Note: n Card No. 1 ~ 6

- After displaying the error contents, it asks whether to clear the error trace data or not.

```
Clear ? ( Y/N ) : =
```

You can clear the error trace data by inputting "Y".

9.8. SAVE COMMAND (PROGRAM/DATA BACK UP)

1. FUNCTION
To back up a certain program or data on the VPS hard disk.

2. OPERAND
Nothing.

3. HOW TO USE, EXAMPLE FOR USAGE

```
$SAVE
Disk Data Down-load (Xmodem )
        1 : Program
        2 : Parameters
        3 : System Prompts
        4 : User Prompts-1
        5 : User Prompts-2
        6 : Custom Service Menus
        7 : Personal Greeting
        8 : Company Greeting
Select No. : =
```

Select the item to be backed up.

```
To start press 'RETURN'
```

Press the return key.

```
_ _ _ _ _ SAVE Start !!
```

To select the data receiving mode (Xmodem) in DTP, point to the name of the file to be backed up. Now it is possible to transfer the data by Xmodem protocol.

Note:
(1) Command cancellation before transfer - '¥' or '\'
(2) Transfer cancellation during receiving - follow your communication software.

Note:
Please refer to another sheet for the details of SAVE command.

9.9. LOAD COMMAND (PROGRAM/DATA UP-DATE)

1. FUNCTION
To update a certain program or data on the VPS hard disk.

2. OPERAND

Nothing.

3. HOW TO USE, EXAMPLE FOR USAGE

```
$LOAD
Disk Data Up-load (Xmodem)
        1 : Program
        2 : Parameters
        3 : System Prompts
        4 : User Prompts-1
        5 : User Prompts-2
        6 : Custom Service Menus
        7 : Personal Greeting
        8 : Company Greeting
Select No. : =
```

Select the item to update.

```
To start press 'RETURN'
```

Press the return key.

```
_ _ _ _ _ LOAD Start !!
```

To select the data receiving mode (Xmodem) in DTP, point to the name of the file for update. Now it is possible to transfer data by Xmodem protocol.

Note:

(1) Command cancellation before transfer - '¥' or ' \ '

(2) Transfer cancellation during receiving - follow your communication soft.

Note:
Please refer to another sheet for the details of LOAD command.

9.10. GPRN (Print All of the VPS Parameters)

1. FUNCTION
Use The GPRN command to print all VPS parameters settings (output to screen).

2. OPERAND
This command is only valid when in the ASCII TERMINAL mode.

3. HOW TO USE, EXAMPLE FOR USAGE
Nothing

```
$ GPRN
    0:  All Parameters
    1:  Mailbox Setting
    2:  Class of Service Setting
    3:  Port/Trunk Service Setting
    4:  Service Setting - Auto Attn. Setting
    5:  Service Setting - Custom Service Setting
    6:  Service Setting - Caller ID Call Routing
    7:  System Parameter Setting - System Group  Assignment
    8:  System Parameter Setting -        Time Service, Holiday, Daylight Saving Time
    9:  System Parameter Setting - Prompt Setting
   10:  System Parameter Setting - System Caller Name Announcement
   11:  System Parameter Setting - Others
   12:  Hardware Setting
   13:  System Reset Clear Parameter

  Please select : =
```

9.11. VERS COMMAND (TO DISPLAY EACH CARD AND PROGRAM VERSION OF HARD DISK)

1. FUNCTION
To display CPU ROM and the program version on the hard disk.

2. OPERAND
Nothing.

3. HOW TO USE, EXAMPLE FOR USAGE

```
$VERS
V.P.S. PROGRAM VERSION
MAIN DISK : VR21AA (3.08) .....(1)
MAIN DISK : VR01AA (1.03) .....(2)
```

[Explanation]

(1) Hard disk - program version display
MAIN DISK : Version (Internal version)

Note: Users do not need to pay attention to <Internal version> .

(2) CPU ROM - program version display
MAIN ROM : Version (Internal version)

9.12. CREP COMMAND (DISPLAY CUSTOM MENU INFORMATION)

1. FUNCTION

To display installed information inside the designated number custom menu.
In case the custom menu is nested, it is displayed in stages (maximum of 8).

2. OPERAND

It is possible to select from 1 to 100 with the custom menu number display.

3. HOW TO USE, EXAMPLE FOR USAGE

```
$ crep 20
Custom   [  20]    ( User-1 ) ( Access :     0 ) ( Menu Msg. : None )
                ↓          ↓          ↓          ↓
       (Remarks 1)  (Remarks 2)  (Remarks 3)  (Remarks 4)
|   < Custom Service Entry Menu > → (Remarks 5)

[1]-Xfer Mbx (401)            → (Remarks 6)

[2]-Xfer Extn (402)           → (Remarks 7)

[3]-Custom [  21]  (System)  (Access :    0)  (Menu Msg. : None)
|        |   < Voice Mail Information Eng. >
|       [1] – Custom [  22]  (User-2)  (Access :    0)  (Menu Msg. : None)
|        |        | < Voice Mail Information Eng. >
|        |       [1]- Operator
|        |       [2]- Name Dial
|        |       [3]- Subscriber
|        |       [4]- Dprt Dial
|        |       [*]- Main Menu
|       [*]-Main Menu
[6]- Operator
[7]- Exit
[8]- Pre. Menu
[*]- Main Menu
[#]- Exit
$
```

Note:
Remarks 1) Custom menu No.
Remarks 2) Prompt kind (System / Use - 1 / User - 2)
Remarks 3) Custom service access number
(How many times this custom menu is accessed by telephone service.)
Remarks 4) The condition of menu message recording (Rec / None)
Remarks 5) Description
Remarks 6) Mail box number
Remarks 7) Extension number

9.13. CCLR COMMAND (TO CLEAR CUSTOM MENU ACCESS NUMBER)

1. FUNCTION
To clear a selected number of custom menu access number. (The number of times custom service number was accessed by telephone service.)

2. OPERAND
It is possible to select from 1 to 100 with the custom menu number to clear.
When 0 is selected, all of the custom menu is cleared.

3. HOW TO USE, EXAMPLE FOR USAGE

```
$ CCLR 20
Custom Menu < 20 > Accessing Counter is Cleared

$ CCLR 0
All Custom Menu Accessing Counters are Cleared
```

9.14. MWL COMMAND (SETTING THE NUMBER OF MESSAGE WAITING LAMP RETRY)

1. FUNCTION
In case the message waiting lamp turn fails to on and off, VPS retries after a certain period. With this command the number of retries can be installed.

2. OPERAND
Nothing.

3. HOW TO USE, EXAMPLE FOR USAGE

```
$MWL
Current Setting of M.W.L. Retry Count is 3
Enter M.W.L. Retry Count (1-3) : =
```

- Select the number of retry (1 ~ 3 times)

9.15. MRL COMMAND (SETTING THE MINIMUM TIME OF MESSAGE

RECORDING)

1. FUNCTION
With this command, the minimum time of message recording can be installed. A message shorter than installed here doesn't seem to be a message, so not be recorded.

2. OPERAND
Nothing.

3. HOW TO USE, EXAMPLE FOR USAGE

```
$MRL
Current Setting of Minimum Recording length is 2
Enter Minimum Recording length (0-3) : =
```

- **Input the recording time by seconds (range: 0 ~ 3 seconds)**
  To input 0 seconds means all recorded messages are effective.

9.16. MPLT COMMAND (DISPLAY REGISTERED USER PROMPT)

1. FUNCTION
To display prompt No. of registered (recorded) user prompt.

2. OPERAND
Nothing.

```
$MPLT
```

3. HOW TO USE, EXAMPLE FOR USAGE

```
$MPLT
   * * *  List of Registered User Prompt 1 No.  ( [1], [2], . . . , [931] )  * * *

     1,    2,    3,    4,    5,    6,    7,    8,    9,   10,   11,   12,   13,   . . .
    21,   22,   23,   24,   25,   26,   27,   28,   29,   30,   31,   32,   33,   . . .
    41,   42,   43,   44,   45,   46,   47,   48,   49,   50,   51,   52,   53,   . . .
    61,   62,   63,   64,   65,   66,   67,   68,   69,   70,   71,   72,   73,   . . .
    81,   82,   83,   84,   85,   86,   87,   88,   89,   90,   91,   92,   93,   . . .
   101,  102,  103,  104,  105,  106,  107,  108,  109,  110,  111,  112,  113,   . . .
      .     .     .     .     .     .     .     .     .     .     .     .     .
      .     .     .     .     .     .     .     .     .     .     .     .     .
      ,     ,     ,     ,     ,     ,     ,     ,     ,     ,     ,     ,     ,   . . .
      ,     ,     ,     ,     ,     ,     ,     ,     ,     ,     ,     ,     ,   . . .

 Total Number Registered  =  419                                          ..... (1)

   * * *  List of Registered User Prompt 2 No.  ( [1], [2], . . . , [931] )  * * *

      ,     ,     ,     ,     ,     ,     ,     ,     ,     ,     ,     ,     ,   . . .
      ,     ,     ,     ,     ,     ,     ,     ,     ,     ,     ,     ,     ,   . . .
      ,     ,     ,     ,     ,     ,     ,     ,     ,     ,     ,     ,     ,   . . .
      .     .     .     .     .     .     .     .     .     .     .     .     .
      .     .     .     .     .     .     .     .     .     .     .     .     .
      ,     ,     ,     ,     ,     ,     ,     ,     ,     ,     ,     ,     ,   . . .
      ,     ,     ,     ,     ,     ,     ,     ,     ,     ,     ,     ,     ,   . . .
      ,     ,     ,     ,     ,     ,     ,     ,     ,     ,     ,     ,     ,   . . .
      ,     ,     ,     ,     ,     ,     ,     ,     ,     ,     ,     ,     ,   . . .

 Total Number Registered  =  0                                            ..... (2)
```

[Explanation]
(1) The total number of registered User Prompt 1.
(2) The total number of registered User Prompt 2.

9.17. QSET COMMAND (QUICK SETUP)

1. FUNCTION
To start Quick Setup.

2. OPERAND
Nothing.

3. HOW TO USE, EXAMPLE FOR USAGE

$QSET
Thereafter, Quick Setup Menu starts.

9.18. LMON COMMAND (CIRCUIT CONDITION DISPLAY)

1. FUNCTION
To display the circuit condition every 1.5 seconds on the screen. Input \ to terminate display. In the case of an ASCII screen, it is displayed only once.

2. OPERAND
Nothing.

3. HOW TO USE, EXAMPLE FOR USAGE

```
$ LMON
 No. : Status                  No. : Status
 1 : Ready                     4 : Ready
 2 : Ready                     5 : Ready
 3 : Ready                     6 : Ready
```

Note:

"Ready"
"Incoming Call"
"Outgoing Call"
"DSP Reset"
"PT Connect"
"Error"

...Possible to serve
...Processing arrival service
...Processing sending service
...Processing DSP reset disposition
...Processing PT connect disposition
...DSP Card is not loaded.

9.19. PUTD (DTMF INFORMATION DISPLAY)

1. FUNCTION
Used to display DTMF tones the VPS is receiving and sending.
In addition to DTMF, the following information is displayed.

A type of Incoming Call Service (Voice Mail, Automated Attendant, Custom Interview) when the caller enters any service.
One " * " means 4 secs while VPS is recording message etc.

2. OPERAND
See 3.

3. HOW TO USE, EXAMPLE FOR USAGE
Once you enter "PUTD", this mode is kept until you enter "PUTD" again.
Default setting of this mode for all ports is "OFF".

```
$ PUTD
Target Port : **** **
Don’t leave enabled after troubleshooting
$
```

If you want to change the mode back to "OFF", enter "PUTD" again.

```
$ PUTD
Target Port : 0000 00
Don’t leave enabled after troubleshooting
$


Note :
" * " means "enable" for the port
"0" means "disable" for the port
```

If you want to set the mode for only one specified port, type "PUTD" and the port number.

```
                    port 1
$ PUTD 1            ↓
Target Port : 0000 0*
Don't leave enabled after troubleshooting
$
```

Sample of display is as follows.

```
$PUTD
Target Port : **** **
Don’t leave enabled after troubleshooting
$
****
[1] DTMF : #
[1] DTMF : 8
[1] A.Attend
[1] DTMF : #
[1] DTMF : 6
[1] Voice Mail
[1] DTMF : 1
[1] DTMF : 0
[1] DTMF : 1
[1] NonSub Svc
[1]
[1] DTMF : D
[1] DTMF : D
 ***
[1] Thank you
```

Warning

1. **"PUTD" is a command originally used for troubleshooting. Do not use in normal use.**
2. **While "PUTD" mode is "ON", do not remove the RS-232C connection be cause the VPS is continuously sending data to the terminal, and it may cause data overflow.**

9.20. WCID (Wait for Caller ID)

1. FUNCTION

Use the WCID command to specify the length of time (in seconds) the VPS must wait for the Caller ID after the VPS has received the incoming call from the PBX.

2. OPERAND

If Caller ID is not needed at all, set the waiting time to “0” to accelerate the VPS respones to incoming calls.

3. HOW TO USE, EXAMPLE FOR USAGE
Nothing

```
$ WCID
   WAIT TIME FOR CALLER ID (5 sec) [0-60 sec] : =0
$
```

9.21. DCLR COMMAND (INITIALIZE PARAMETER, DATA OF HARD DISK)

1. FUNCTION
To clear the parameter or data of the selected drive's hard disk.
The following is to be cleared.
- Each parameter (Mail box information, report information, etc.)
- Voice data (system guidance, user guidance, message, etc.)
After execution, VPS should start up again.

2. OPERAND

$DCLR [drv], [opt]

(1) [drv]
Select drive No.
1 : Drive 1
2 : Drive 2
(2) [opt] (Option)
Select the parameter and data to be cleared.
0 : Install hard disk to system disk, then clear all parameters and voice data.
3 : Install hard disk to system disk, then all parameters and voice data, except for user guidance.
In this case, install target disk to drive 1. (Namely to select [drv] = 1) (1)
4 : Clear all voice data except for user guidance.
In this case, install target disk to drive 1. (Namely to select [drv] = 1) (1)
5 : Clear user guide only.
In this case, install target disk to drive 1. (Namely to select [drv] = 1) (1)

3. HOW TO USE, EXAMPLE FOR USAGE
Example is shown blow.

```
$DCLR 1, 0 .....(1)
 Please POWER OFF !.....(2)
$DCLR 2, 3.....(3)
 Please POWER OFF !
$DCLR 1, 4.....(4)
 Please POWER OFF !
```

[Explanation]
(1) To clear all parameters and voice data in drive 1.
(2) To display the message urges to start up VPS again.
It won't accept key input at all. Turn the power off and then on.
(3) To clear all voice data except user prompt in drive 2.
(4) To clear all user prompts in drive 1 and user prompt 2.

9.22. DCPY COMMAND (ALL SELECTOR COPIES BETWEEN DRIVES)

1. FUNCTION
To copy the data (all sector) in drive No. 1 to drive No. 2.

2. OPERAND
Nothing.

3. HOW TO USE, EXAMPLE FOR USAGE

```
$DCPY
001234.....(1)
$ .....(2)
```

[Explanation]
(1) To display the sector number of present copying.
(2) To display command prompt "$".
It means copy finishes normally.

Note:
When an error caused by the hard disk occurs during execution of DCPY, the error sector number is displayed. The sector is skipped, then disposition continues. It is recommended to check the sector with the RECO command and execute recover after DCPY finishes. Concerning the RECO command, please refer to <Chapter 8 8.7 RECO command>.
The following are the commands displayed during error sector copying.

- DCPY

- PCPY
- GCPY
- XCPY
- SYSD

9.23. PCPY COMMAND (PROGRAM COPY BETWEEN DRIVES)

1. FUNCTION
To copy the VPS program in drive No.1 to the program region of drive No.2.

2. OPERAND
Nothing.

3. HOW TO USE, EXAMPLE FOR USAGE

```
$PCPY
 001234.....(1)
$ .....(2)
```

[Explanation]
(1) Sector number presently copying.
(2) To display Command prompt "$".

9.24. GCPY COMMAND (SYSTEM GUIDANCE COPY BETWEEN DRIVES)

1. FUNCTION
To copy system guidance in drive No.1 to drive No.2.

2. OPERAND
Nothing.

3. HOW TO USE, EXAMPLE FOR USAGE

```
$GCPY
 001234.....(1)
$ .....(2)
```

[Explanation]
(1) Sector number presently copying.
(2) To display Command prompt "$".

9.25. XCPY COMMAND (COPY FROM DRIVE NO. 2 TO DRIVE NO. 1)

1. FUNCTION
To copy from drive No.2 to drive No. 1. The following are copy objects.
(1) Program
(2) System guidance
(3) User prompt

2. OPERAND

```
$XCPY [para]
```

(1) [para]
Nothing : Program, System guidance copy (Drive 2 → Drive 1)
1 : Program copy (Drive 2 → Drive 1)
2 : System guidance copy (Drive 2 → Drive 1)
3 : User prompt copy (Drive 2 → Drive 1)

3. HOW TO USE, EXAMPLE FOR USAGE

```
$XCPY.....(1)
 001234.....(2)
$ .....(3)
$XCPY 3.....(4)
 XCPY (User-Prompt Copy Disk2 -> Disk1) Start !.....(5)
 001234
 XCPY (User-Prompt Copy Disk2 -> Disk1) End !.....(6)
 * * * Total Copy Number : 125 * * *.....(7)
$
```

[Explanation]
(1) To copy program and system guidance.
(2) To display sector number presently copying.
(3) To display command prompt "$".
Copy ends normally.
(4) To copy user prompt.
(5) To display copy starts.
(6) To display copy ends.

(7) To display the user prompt's total number copies.

9.26. SYSD COMMAND (INSTALL DRIVE 2 TO SYSTEM DISK)

1. FUNCTION
The Following jobs are required to install Drive No.2 to a system disk.
(1) To initialize Drive 2. (FORMAT 2)
(2) To clear Drive 2. (DCLR 2, 0)
(3) To copy program from Drive 1 to Drive 2.
To copy system guidance from Drive 1 to Drive 2.
To copy user prompt from Drive 1 to Drive 2.
During this operation you can choose to copy-only user prompt 1 or only user prompt 2 or both user prompt 1 and 2. (To put coming up prompt No. in order, then store in Drive 2.)

2. OPERAND
Nothing.

3. HOW TO USE, EXAMPLE FOR USAGE

```
$SYSD
 Select User Prompt No. ( 0-2, 9 )
 Ex. If you select No. 1,
 Only User Prompt 1 is copied from Disk1 to Disk2.
 0 : User-1 & User-2
 1 : User-1
 2 : User-2
 9 : Not Copy User Prompt = => 2
 The record time will be set to 32 hours.
 Are you sure?[Y/N]=Y
 * * * FORMAT * * *.....(1)
 * * * DCLR * * *.....(2)
 * * * * * * * * * * * * * * *
 * * * COPY * * *.....(3)
 0005A0
 0020a0
 * * * USRP COPY* * *.....(4)
$.....(5)
```

[Explanation]
(1) Disk 2 format.
(2) To initialize disk 2. (To initialize each table information)
To be displayed every time each table is initialized.
(3) To copy program/ system guidance.

Sector No. copying at present is displayed in real time.
(4) User prompt's copy.
(5) To display command prompt "$".
Copy finishes normally.

9.27. EMDM COMMAND (EXTERNAL MODEM SETUP)

1. FUNCTION
Used to specify modem commands you want to send to external modem connected with VPS.

2. OPERAND
Nothing

3. HOW TO USE, EXAMPLE FOR USAGE
You can set up to 5 AT commands and comment (information) for each command.
This command has a default value for zoom modem in No.1 area.

```
$ emdm

Current AT Commands for External Modem is as follows.
 No.1 Comment : ZOOM
     Command : AT&D0&K0&Q0\N1%C0Q1S0=1&W0

Please enter command number you want to change.
  If you want to initialize all data, enter 0 :=1
===== Command No.1 =====
Enter Comment(Max:32 Characters) =>TEST  <---------- Comment
Enter Command(Max:60 Characters) =>ATQ1&K0S0 <-- Modem Command

Current AT Commands for External Modem is as follows.
 No.1 Comment : test
     Command : ATQ1&K0S0

Please enter command number you want to change.
  If you want to initialize all data, enter 0 :=

       To send the AT commands,
        1.Connect Modem and VPS using RS232C Straight Cable
        2.Access System Manager Service
              and press 9 + Command No. during the Top Menu
               Ex.*999 + 91 ( to send Command No.1 )

$
```

- Modem Command Example
ATE0Q1&D0&S0 = 1&K0&Q0%C0

E0 : Commands are not echoed

Q1 : Disable responses to PC
&D0 : Ignore DTR signal
&S0=1 : DSR always ON (auto answer ON)
&K0 : Disables flow control
&Q0 : Select direct asynchronous mode
%C0 : Data compression disable

The modem commands for connecting with VPS vary with the modem maker.
Please check the manual of the modem.

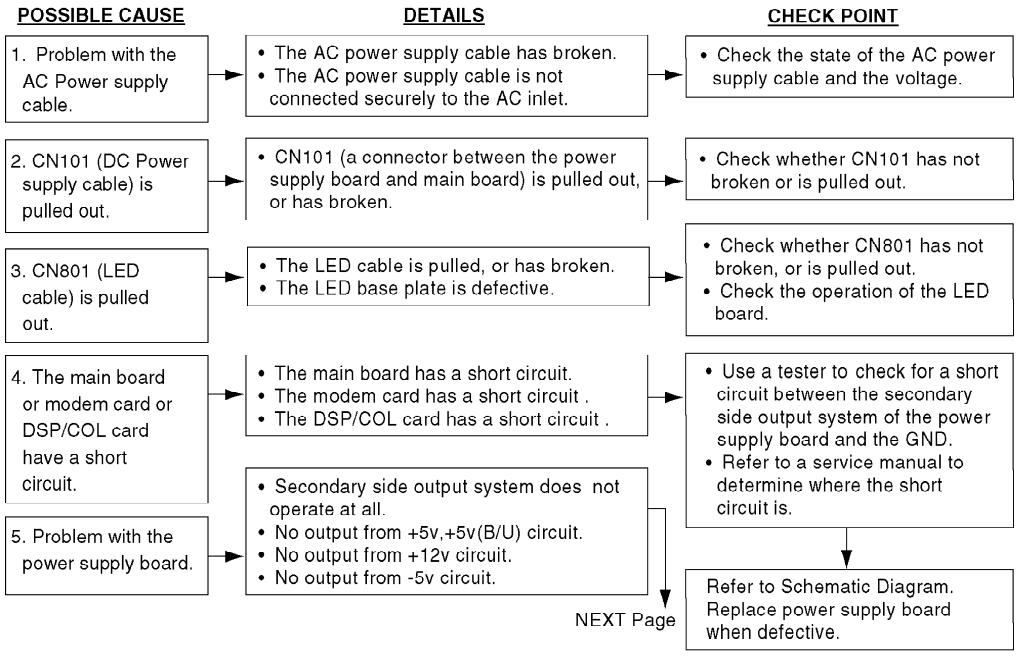
How to send the Modem Command to external modem
Please connect RS-232C straight cable between VPS and modem.

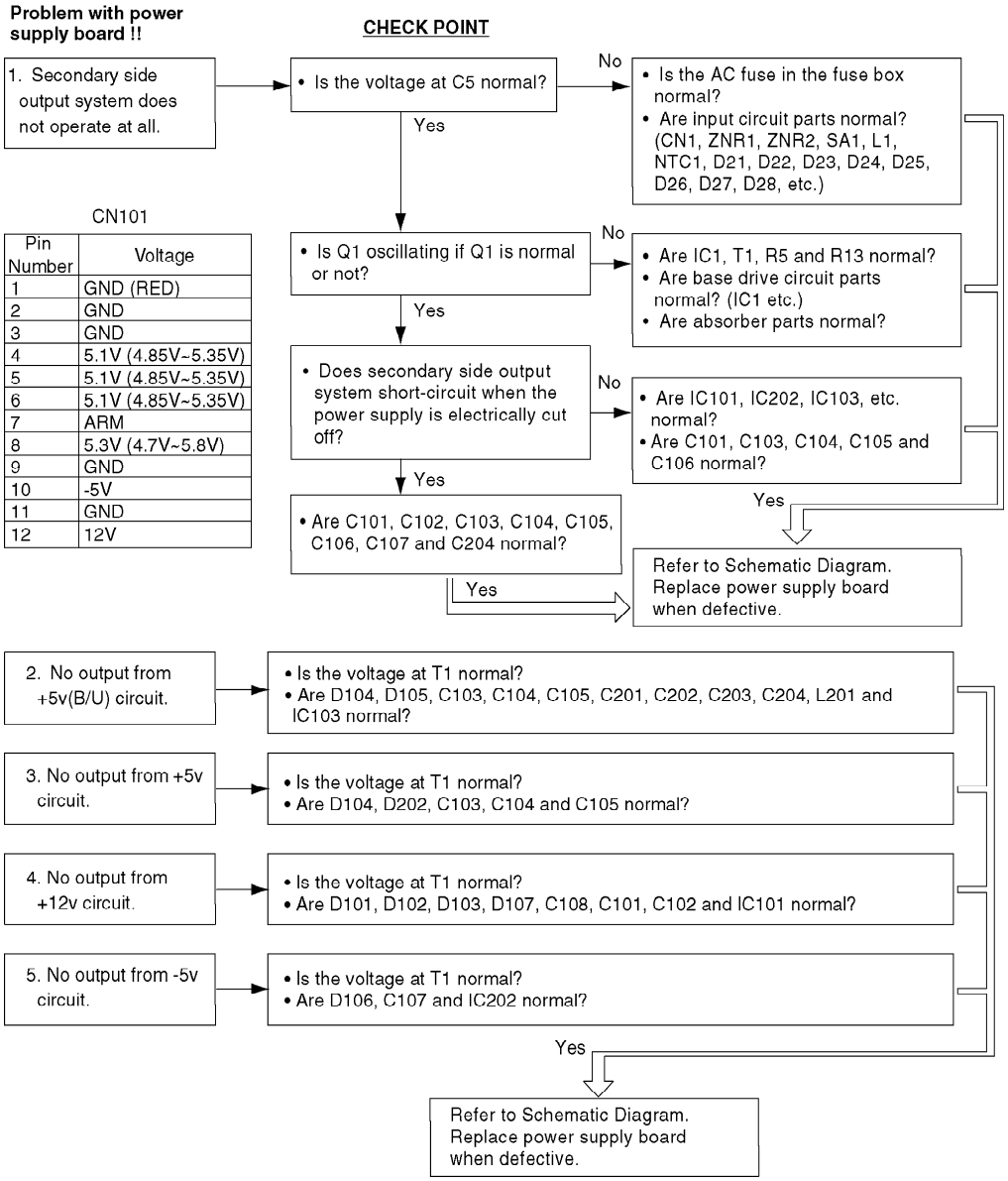
Note:
You have to turn "PUTD" mode back to "OFF" if you already set the mode "ON" for trouble shooting.

To send the command, please access System Manager Service, and enter 9 + No. during the top menu.
For example, *999 + 91 (← VPS sends AT Command No.1).
After sending AT Command, VPS beeps out for about 2 sec.

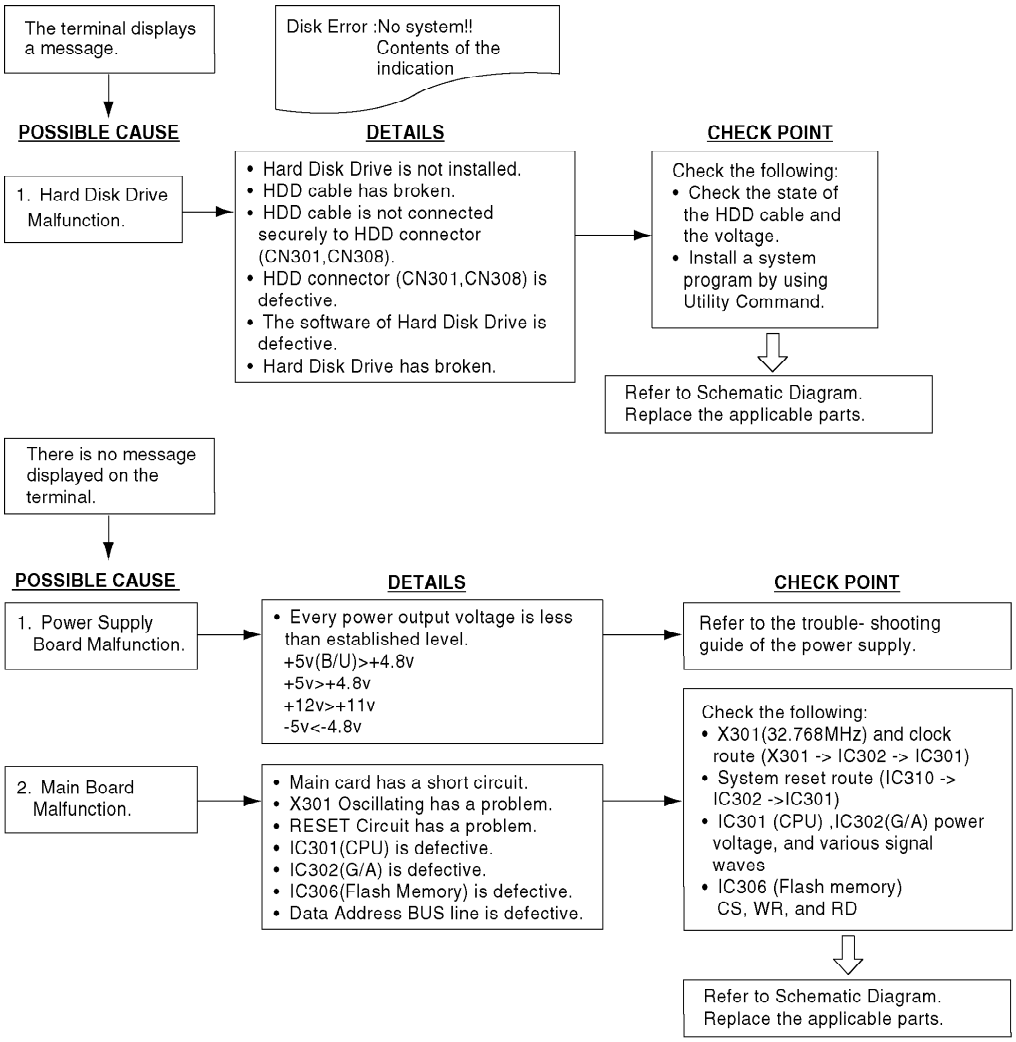
10. TROUBLESHOOTING GUIDE

10.1. THE POWER INDICATOR DOES NOT LIGHT UP WHEN THE POWER SWITCH IS TURNED ON


POSSIBLE CAUSE
DETAILS
CHECK POINT
1. Problem with the AC Power supply cable.
• The AC power supply cable has broken.
• The AC power supply cable is not connected securely to the AC inlet.
• Check the state of the AC power supply cable and the voltage.
2. CN101 (DC Power supply cable) is pulled out.
• CN101 (a connector between the power supply board and main board) is pulled out, or has broken.
• Check whether CN101 has not broken or is pulled out.
3. CN801 (LED cable) is pulled out.
• The LED cable is pulled, or has broken.
• The LED base plate is defective.
• Check whether CN801 has not broken, or is pulled out.
• Check the operation of the LED board.
4. The main board or modem card or DSP/COL card have a short circuit.
• The main board has a short circuit.
• The modem card has a short circuit .
• The DSP/COL card has a short circuit .
• Use a tester to check for a short circuit between the secondary side output system of the power supply board and the GND.
• Refer to a service manual to determine where the short circuit is.
5. Problem with the power supply board.
• Secondary side output system does not operate at all.
• No output from +5v,+5v(B/U) circuit.
• No output from +12v circuit.
• No output from -5v circuit.
Refer to Schematic Diagram. Replace power supply board when defective.
NEXT Page


Problem with power supply board !!
CHECK POINT
1. Secondary side output system does not operate at all.
• Is the voltage at C5 normal?
No
• Is the AC fuse in the fuse box normal?
• Are input circuit parts normal? (CN1, ZNR1, ZNR2, SA1, L1, NTC1, D21, D22, D23, D24, D25, D26, D27, D28, etc.)
Yes
CN101
Pin Number
Voltage
1 GND (RED)
2 GND
3 GND
4 5.1V (4.85V~5.35V)
5 5.1V (4.85V~5.35V)
6 5.1V (4.85V~5.35V)
7 ARM
8 5.3V (4.7V~5.8V)
9 GND
10 -5V
11 GND
12 12V
• Is Q1 oscillating if Q1 is normal or not?
No
• Are IC1, T1, R5 and R13 normal?
• Are base drive circuit parts normal? (IC1 etc.)
• Are absorber parts normal?
Yes
• Does secondary side output system short-circuit when the power supply is electrically cut off?
No
• Are IC101, IC202, IC103, etc. normal?
• Are C101, C103, C104, C105 and C106 normal?
Yes
• Are C101, C102, C103, C104, C105, C106, C107 and C204 normal?
Yes
Yes
Refer to Schematic Diagram. Replace power supply board when defective.
2. No output from +5v(B/U) circuit.
• Is the voltage at T1 normal?
• Are D104, D105, C103, C104, C105, C201, C202, C203, C204, L201 and IC103 normal?
3. No output from +5v circuit.
• Is the voltage at T1 normal?
• Are D104, D202, C103, C104 and C105 normal?
4. No output from +12v circuit.
• Is the voltage at T1 normal?
• Are D101, D102, D103, D107, C108, C101, C102 and IC101 normal?
5. No output from -5v circuit.
• Is the voltage at T1 normal?
• Are D106, C107 and IC202 normal?
Yes
Refer to Schematic Diagram. Replace power supply board when defective.

10.2. THE VPS SYSTEM DOES NOT START OPERATING


The terminal displays a message.
Disk Error :No system!!
Contents of the indication
POSSIBLE CAUSE
DETAILS
CHECK POINT
1. Hard Disk Drive Malfunction.
• Hard Disk Drive is not installed.
• HDD cable has broken.
• HDD cable is not connected securely to HDD connector (CN301,CN308).
• HDD connector (CN301,CN308) is defective.
• The software of Hard Disk Drive is defective.
• Hard Disk Drive has broken.
Check the following:
• Check the state of the HDD cable and the voltage.
• Install a system program by using Utility Command.
Refer to Schematic Diagram.
Replace the applicable parts.
There is no message displayed on the terminal.
POSSIBLE CAUSE
DETAILS
CHECK POINT
1. Power Supply Board Malfunction.
• Every power output voltage is less than established level.
+5v(B/U)>+4.8v
+5v>+4.8v
+12v>+11v
-5v<-4.8v
Refer to the trouble- shooting guide of the power supply.
2. Main Board Malfunction.
• Main card has a short circuit.
• X301 Oscillating has a problem.
• RESET Circuit has a problem.
• IC301(CPU) is defective.
• IC302(G/A) is defective.
• IC306(Flash Memory) is defective.
• Data Address BUS line is defective.
Check the following:
• X301(32.768MHz) and clock route (X301 -> IC302 -> IC301)
• System reset route (IC310 -> IC302 ->IC301)
• IC301 (CPU) ,IC302(G/A) power voltage, and various signal waves
• IC306 (Flash memory) CS, WR, and RD
Refer to Schematic Diagram.
Replace the applicable parts.

10.3. BLINKING DOES NOT STOP ALTHOUGH THE VPS SYSTEM HAS ALREADY OPERATED

Blinking Pattern of Power indicator (RED LED) <System initialize>

VPS SYSTEM CONDITIONS	DATA TERMINAL SCREEN	BLINKING SEQUENCE OF THE POWER INDICATOR
1.Power UP		Light ON
2.Diagnostics	CARD TEST	Blinking Repeat 0.25sec ON and 0.25sec OFF
3.initialize	SYSTEM SETUP 1…2…3…	Blinking Repeat 0.25sec ON and 0.25sec OFF
4.Operation	* * ON LINE MODE * *	Light ON
5.Warning Error	* * OFF LINE MODE * *	Blinking Repeat 0.5sec ON and 0.5sec OFF
6.Fatal Error	* * OFF LINE MODE * *	Blinking Repeat 0.5sec ON and 3.5sec OFF

5.Warning Error

POSSIBLE CAUSE	DETAILS	CHECK POINT
1. There is an error in the integration setup with the PBX.	• Connect terminal and re-check the integration setup with the PBX. • Recheck the Voice Mail Integration on the PBX side. • Refer to the guide of Problem 4, 5 and check the circuit.	Refer to the setting up manual to recheck the integration with the PBX.
2. Malfunction in the Interface circuit.		

6.Fatal Error

POSSIBLE CAUSE	DETAILS	CHECK POINT
1. DSP card Malfunction.	• DSP card is defective. • Circuit to access DSP card is defective.	Check the following: • IC109-53pin(4.096MHz) • IC109-37,47pin (14.366MHz) • IC109-39pin /RS(H) • IC109 /DS, /STRB, R/W

Blinking Pattern of Power indicator (RED LED) <Self Diagnostics>

ERROR TYPE	DATA TERMINAL SCREEN	BLINKING SEQUENCE OF THE POWER INDICATOR (No. of blinks in a 6 second interval.)
1.RAM Error	RAM R/W ERROR	The Indicator blinks 2 times
2. ROM Error	ROM ERROR Sum Error!!	The Indicator blinks 3 times
3. HDD Error (case-1)	DISK ERROR Initialize Error!!	The Indicator blinks 4 times
4. HDD Error (case-2)	DISK ERROR No System!!	The Indicator blinks 5 times
5. HDD Error (case-3)	DISK ERROR Program Load Error!!	The Indicator blinks 6 times
6. HDD Error (case-4)	DISK ERROR Program Sum Error!!	The Indicator blinks 7 times

1.RAM Error

POSSIBLE CAUSE	DETAILS	CHECK POINT
1.RAM Malfunction.	• RAM is defective. • Circuit to access RAM is defective.	Check the following: • IC331,IC332 CS, WE, OE • DATA BUS ADDRESS BUS

2. ROM Error

POSSIBLE CAUSE	DETAILS	CHECK POINT
1.Program of the System Flash Memory (IC306) is defective.	• Program in System Flash Memory is defective. • Program in System Flash Memory is not compatible with the Version of Hard Disk Drive.	Replace the System Flash Memory.

3. HDD Error (case-1)

POSSIBLE CAUSE	DETAILS	CHECK POINT
1. HDD cable is pulled out.	• HDD cable (a cable between the Hard Disk Drive and main board) is pulled out , or has broken.	• Check whether HDD cable has not broken or is pulled out.

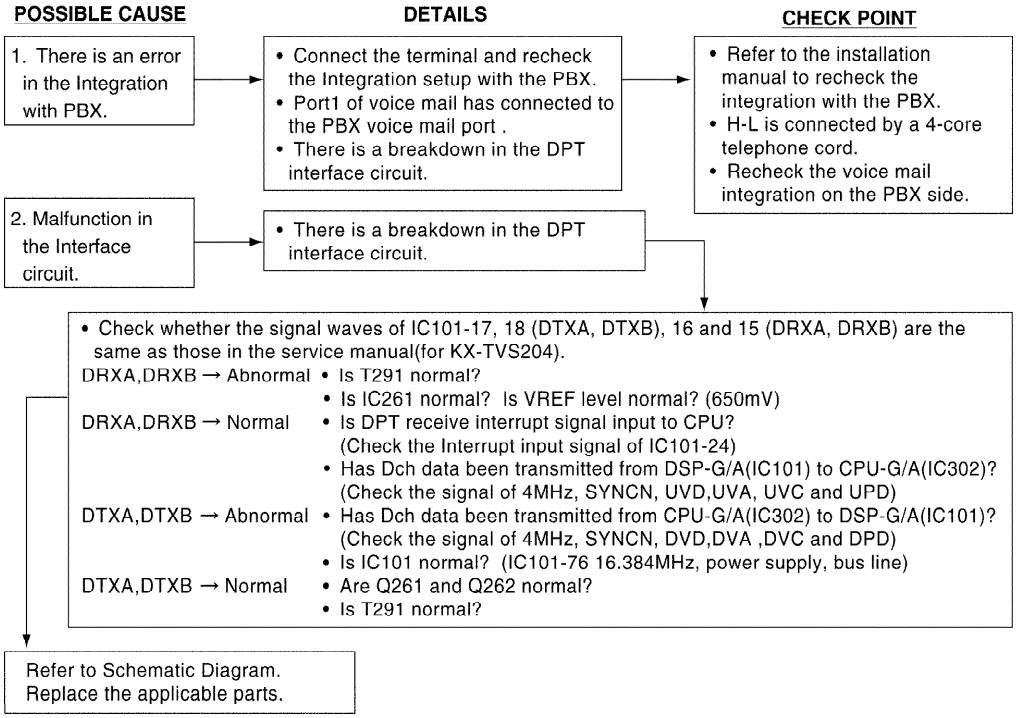
4. HDD Error (case-2)

POSSIBLE CAUSE	DETAILS	CHECK POINT
1. System program is not installed.	• System program is not installed to the Hard Disk Drive.	• Install system program to the Hard Disk Drive.

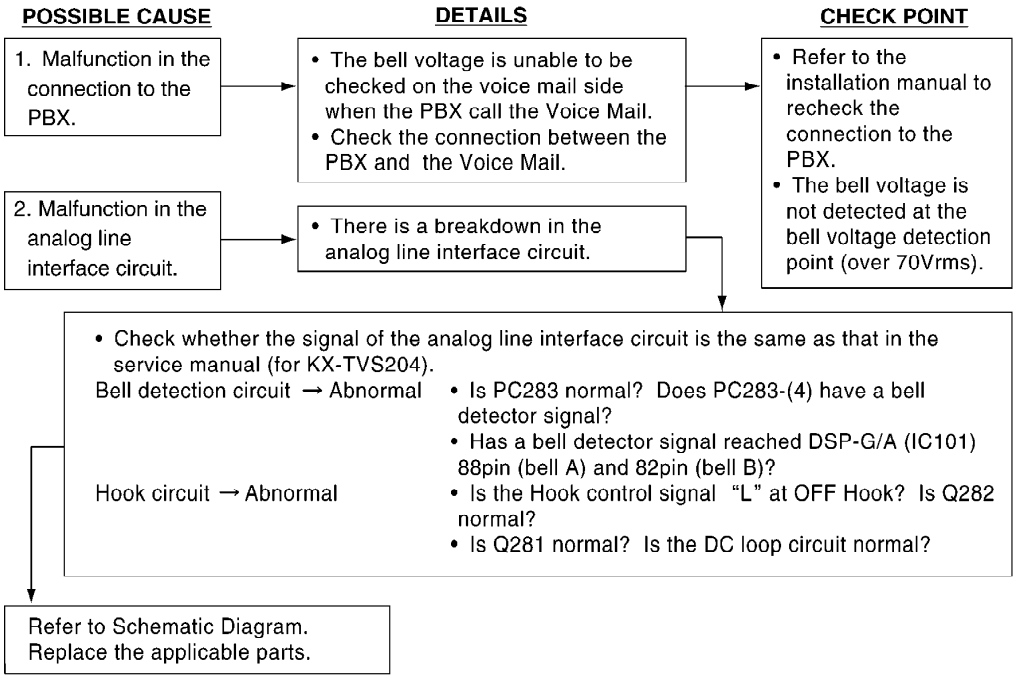
5. HDD Error (case-3)
6. HDD Error (case-4)

POSSIBLE CAUSE	DETAILS	CHECK POINT
1. Program loading from Hard Disk Drive to System Flash Memory (IC306) fails.	• Hard Disk Drive is defective. • Hard Disk Drive can not be recognized. • Write action to System Flash Memory IC306 has a problem.	Check the following: • The Hard Disk Drive (Refer to Problem2) • IC306 RESET(H), CE, WE • The Hard Disk Drive control system

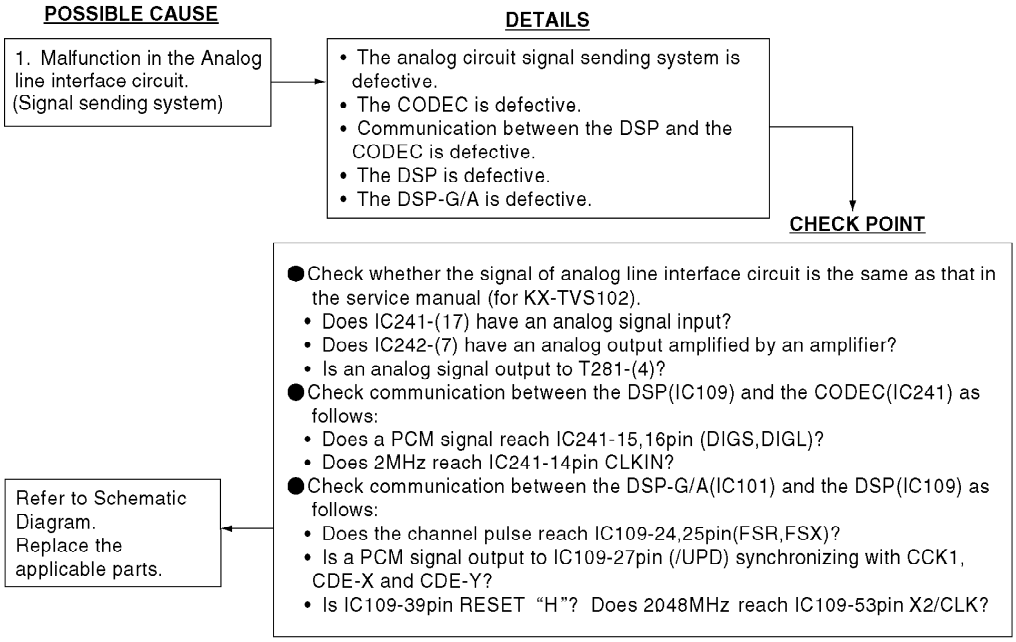
10.4. DPT INTEGRATION CONNECTION BETWEEN VOICE MAIL AND TD SERIES PBX FAILS


POSSIBLE CAUSE
DETAILS
CHECK POINT
1. There is an error in the Integration with PBX.
• Connect the terminal and recheck the Integration setup with the PBX.
• Port1 of voice mail has connected to the PBX voice mail port .
• There is a breakdown in the DPT interface circuit.
• Refer to the installation manual to recheck the integration with the PBX.
• H-L is connected by a 4-core telephone cord.
• Recheck the voice mail integration on the PBX side.
2. Malfunction in the Interface circuit.
• There is a breakdown in the DPT interface circuit.
• Check whether the signal waves of IC101-17, 18 (DTXA, DTXB), 16 and 15 (DRXA, DRXB) are the same as those in the service manual(for KX-TVS204).
DRXA,DRXB → Abnormal
• Is T291 normal?
• Is IC261 normal? Is VREF level normal? (650mV)
DRXA,DRXB → Normal
• Is DPT receive interrupt signal input to CPU? (Check the Interrupt input signal of IC101-24)
• Has Dch data been transmitted from DSP-G/A(IC101) to CPU-G/A(IC302)? (Check the signal of 4MHz, SYNCN, UVD,UVA, UVC and UPD)
DTXA,DTXB → Abnormal
• Has Dch data been transmitted from CPU-G/A(IC302) to DSP-G/A(IC101)? (Check the signal of 4MHz, SYNCN, DVD,DVA ,DVC and DPD)
• Is IC101 normal? (IC101-76 16.384MHz, power supply, bus line)
DTXA,DTXB → Normal
• Are Q261 and Q262 normal?
• Is T291 normal?
Refer to Schematic Diagram.
Replace the applicable parts.

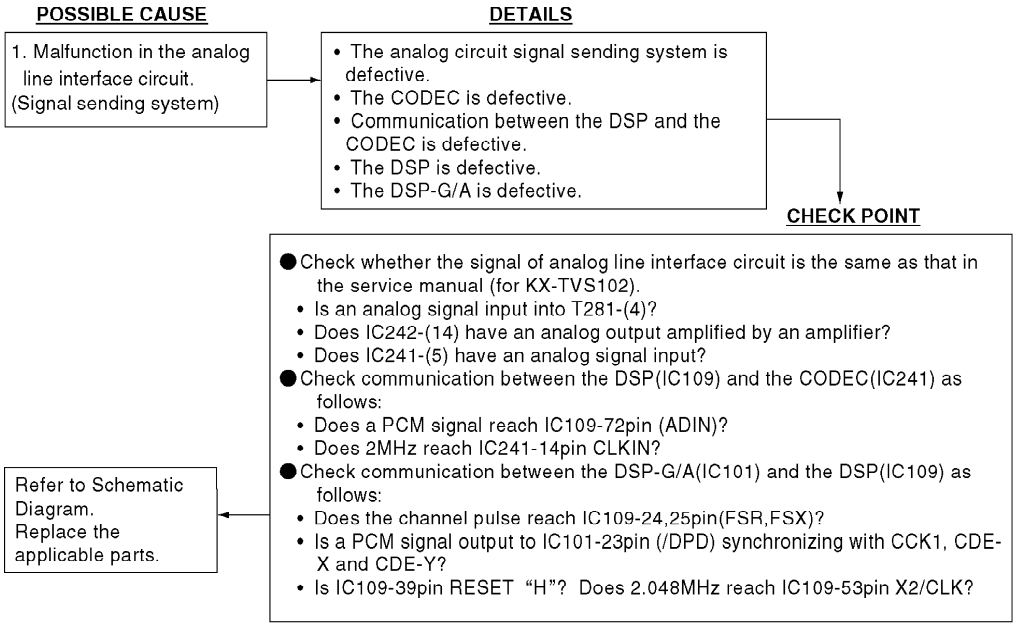
10.5. BELL ARRIVAL AND HOOKING FAIL


POSSIBLE CAUSE
DETAILS
CHECK POINT
1. Malfunction in the connection to the PBX.
• The bell voltage is unable to be checked on the voice mail side when the PBX call the Voice Mail.
• Check the connection between the PBX and the Voice Mail.
• Refer to the installation manual to recheck the connection to the PBX.
• The bell voltage is not detected at the bell voltage detection point (over 70Vrms).
2. Malfunction in the analog line interface circuit.
• There is a breakdown in the analog line interface circuit.
• Check whether the signal of the analog line interface circuit is the same as that in the service manual (for KX-TVS204).
Bell detection circuit → Abnormal
• Is PC283 normal? Does PC283-(4) have a bell detector signal?
• Has a bell detector signal reached DSP-G/A (IC101) 88pin (bell A) and 82pin (bell B)?
Hook circuit → Abnormal
• Is the Hook control signal "L" at OFF Hook? Is Q282 normal?
• Is Q281 normal? Is the DC loop circuit normal?
Refer to Schematic Diagram.
Replace the applicable parts.

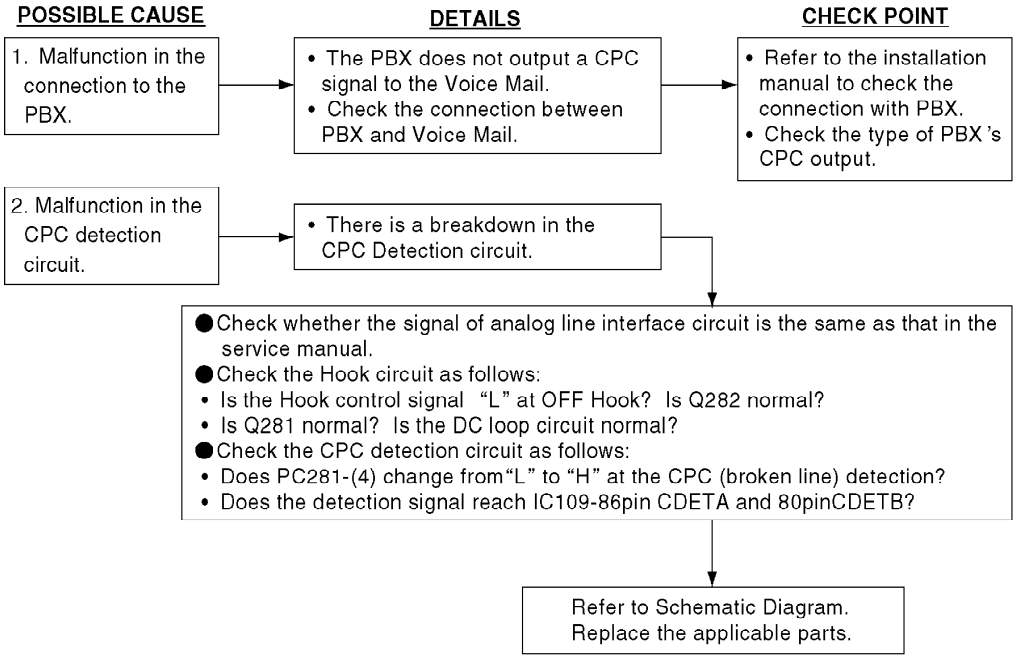
10.6. YOU ARE UNABLE TO HEAR THE GUIDANCE (SLT INTERFACE)


POSSIBLE CAUSE
DETAILS
1. Malfunction in the Analog line interface circuit. (Signal sending system)
• The analog circuit signal sending system is defective.
• The CODEC is defective.
• Communication between the DSP and the CODEC is defective.
• The DSP is defective.
• The DSP-G/A is defective.
CHECK POINT
●Check whether the signal of analog line interface circuit is the same as that in the service manual (for KX-TVS102).
• Does IC241-(17) have an analog signal input?
• Does IC242-(7) have an analog output amplified by an amplifier?
• Is an analog signal output to T281-(4)?
●Check communication between the DSP(IC109) and the CODEC(IC241) as follows:
• Does a PCM signal reach IC241-15,16pin (DIGS,DIGL)?
• Does 2MHz reach IC241-14pin CLKIN?
●Check communication between the DSP-G/A(IC101) and the DSP(IC109) as follows:
• Does the channel pulse reach IC109-24,25pin(FSR,FSX)?
• Is a PCM signal output to IC109-27pin (/UPD) synchronizing with CCK1, CDE-X and CDE-Y?
• Is IC109-39pin RESET "H"? Does 2048MHz reach IC109-53pin X2/CLK?
Refer to Schematic Diagram. Replace the applicable parts.

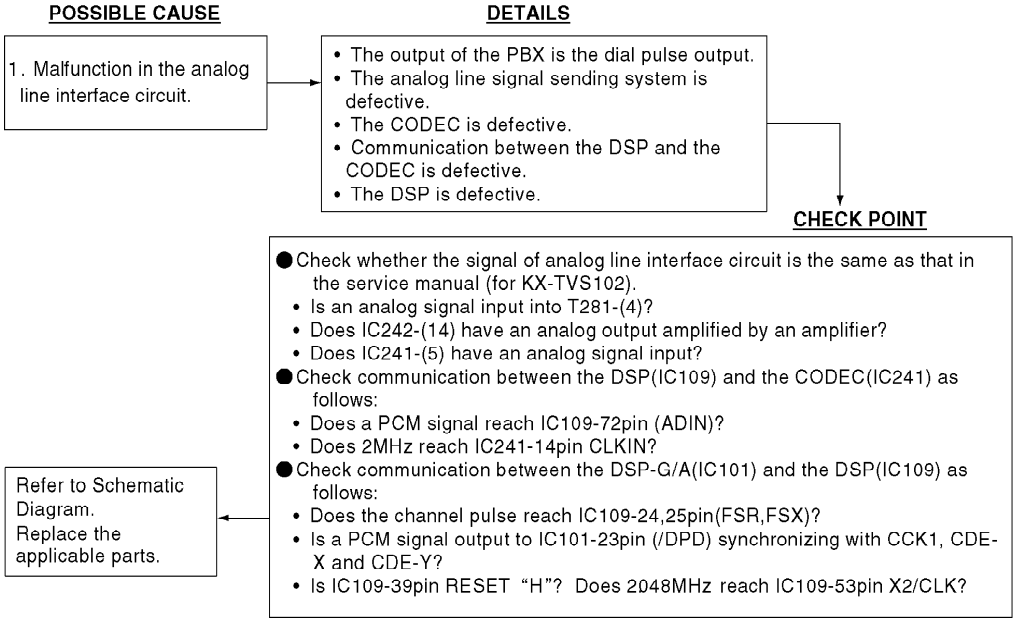
10.7. RECORDING AND REPLAYING MESSAGES FAIL (SLT INTERFACE)


POSSIBLE CAUSE
DETAILS
1. Malfunction in the analog line interface circuit. (Signal sending system)
• The analog circuit signal sending system is defective.
• The CODEC is defective.
• Communication between the DSP and the CODEC is defective.
• The DSP is defective.
• The DSP-G/A is defective.
CHECK POINT
●Check whether the signal of analog line interface circuit is the same as that in the service manual (for KX-TVS102).
• Is an analog signal input into T281-(4)?
• Does IC242-(14) have an analog output amplified by an amplifier?
• Does IC241-(5) have an analog signal input?
●Check communication between the DSP(IC109) and the CODEC(IC241) as follows:
• Does a PCM signal reach IC109-72pin (ADIN)?
• Does 2MHz reach IC241-14pin CLKIN?
●Check communication between the DSP-G/A(IC101) and the DSP(IC109) as follows:
• Does the channel pulse reach IC109-24,25pin(FSR,FSX)?
• Is a PCM signal output to IC101-23pin (/DPD) synchronizing with CCK1, CDE-X and CDE-Y?
• Is IC109-39pin RESET "H"? Does 2.048MHz reach IC109-53pin X2/CLK?
Refer to Schematic Diagram. Replace the applicable parts.

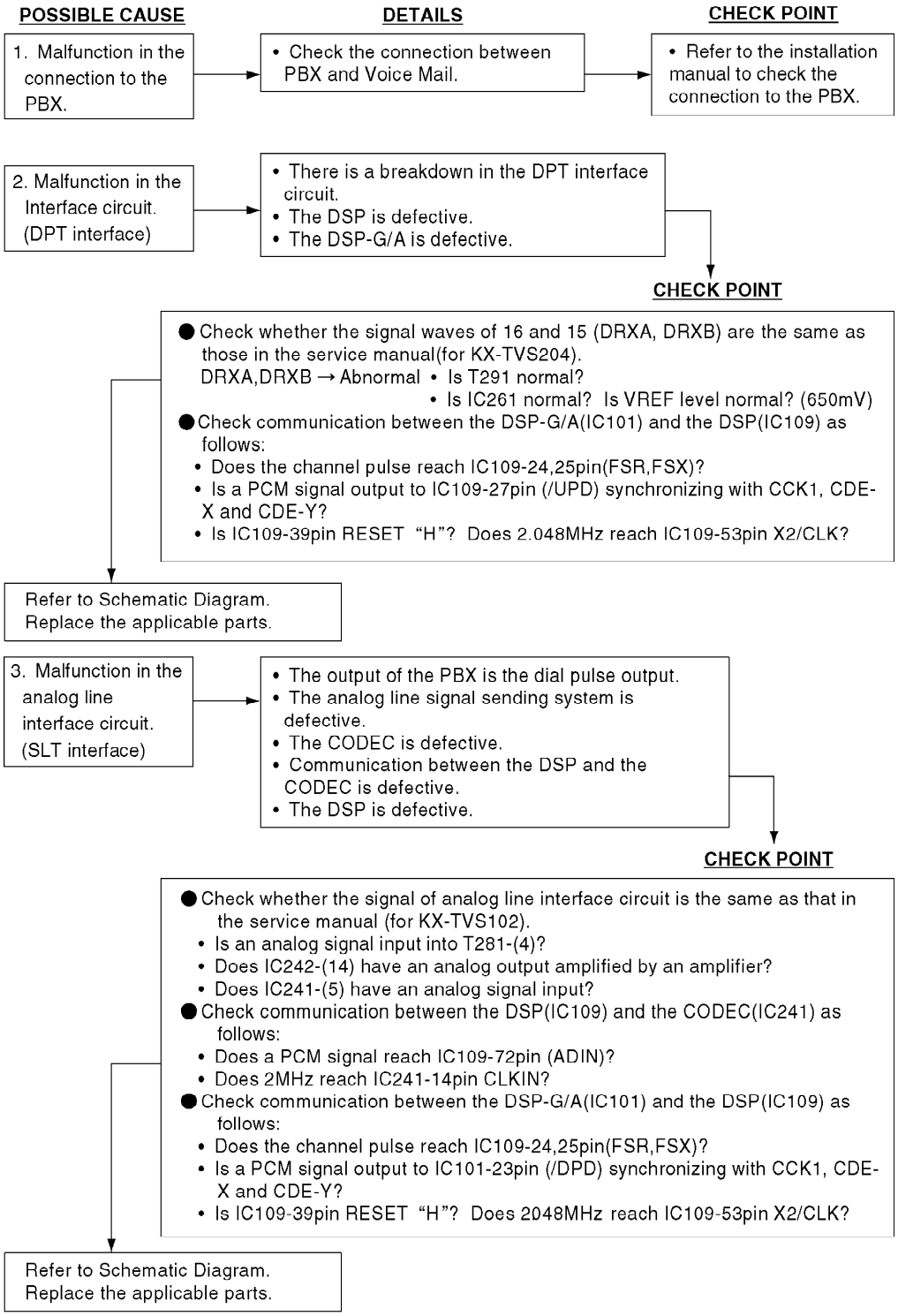
10.8. CPC DETECTION DOES NOT OPERATE (SLT INTERFACE)


POSSIBLE CAUSE
DETAILS
CHECK POINT
1. Malfunction in the connection to the PBX.
• The PBX does not output a CPC signal to the Voice Mail.
• Check the connection between PBX and Voice Mail.
• Refer to the installation manual to check the connection with PBX.
• Check the type of PBX 's CPC output.
2. Malfunction in the CPC detection circuit.
• There is a breakdown in the CPC Detection circuit.
● Check whether the signal of analog line interface circuit is the same as that in the service manual.
● Check the Hook circuit as follows:
• Is the Hook control signal "L" at OFF Hook? Is Q282 normal?
• Is Q281 normal? Is the DC loop circuit normal?
● Check the CPC detection circuit as follows:
• Does PC281-(4) change from"L" to "H" at the CPC (broken line) detection?
• Does the detection signal reach IC109-86pin CDETA and 80pinCDETB?
Refer to Schematic Diagram.
Replace the applicable parts.

10.9. DTMF DETECTION DOES NOT OPERATE (SLT INTERFACE)

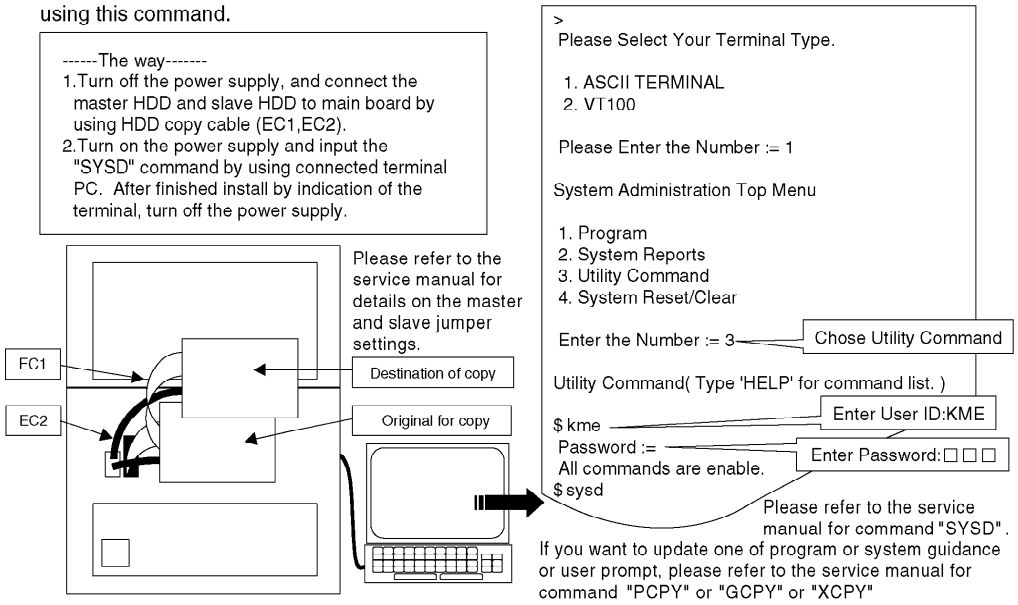

POSSIBLE CAUSE
DETAILS
1. Malfunction in the analog line interface circuit.
• The output of the PBX is the dial pulse output.
• The analog line signal sending system is defective.
• The CODEC is defective.
• Communication between the DSP and the CODEC is defective.
• The DSP is defective.
CHECK POINT
● Check whether the signal of analog line interface circuit is the same as that in the service manual (for KX-TVS102).
• Is an analog signal input into T281-(4)?
• Does IC242-(14) have an analog output amplified by an amplifier?
• Does IC241-(5) have an analog signal input?
● Check communication between the DSP(IC109) and the CODEC(IC241) as follows:
• Does a PCM signal reach IC109-72pin (ADIN)?
• Does 2MHz reach IC241-14pin CLKIN?
● Check communication between the DSP-G/A(IC101) and the DSP(IC109) as follows:
• Does the channel pulse reach IC109-24,25pin(FSR,FSX)?
• Is a PCM signal output to IC101-23pin (/DPD) synchronizing with CCK1, CDE-X and CDE-Y?
• Is IC109-39pin RESET "H"? Does 2048MHz reach IC109-53pin X2/CLK?
Refer to Schematic Diagram.
Replace the applicable parts.

10.10. FAX TONE DETECTION DOES NOT OPERATE


POSSIBLE CAUSE
DETAILS
CHECK POINT
1. Malfunction in the connection to the PBX.
• Check the connection between PBX and Voice Mail.
• Refer to the installation manual to check the connection to the PBX.
2. Malfunction in the Interface circuit. (DPT interface)
• There is a breakdown in the DPT interface circuit.
• The DSP is defective.
• The DSP-G/A is defective.
CHECK POINT
● Check whether the signal waves of 16 and 15 (DRXA, DRXB) are the same as those in the service manual(for KX-TVS204).
DRXA,DRXB → Abnormal • Is T291 normal?
• Is IC261 normal? Is VREF level normal? (650mV)
● Check communication between the DSP-G/A(IC101) and the DSP(IC109) as follows:
• Does the channel pulse reach IC109-24,25pin(FSR,FSX)?
• Is a PCM signal output to IC109-27pin (/UPD) synchronizing with CCK1, CDE-X and CDE-Y?
• Is IC109-39pin RESET "H"? Does 2.048MHz reach IC109-53pin X2/CLK?
Refer to Schematic Diagram.
Replace the applicable parts.
3. Malfunction in the analog line interface circuit. (SLT interface)
• The output of the PBX is the dial pulse output.
• The analog line signal sending system is defective.
• The CODEC is defective.
• Communication between the DSP and the CODEC is defective.
• The DSP is defective.
CHECK POINT
● Check whether the signal of analog line interface circuit is the same as that in the service manual (for KX-TVS102).
• Is an analog signal input into T281-(4)?
• Does IC242-(14) have an analog output amplified by an amplifier?
• Does IC241-(5) have an analog signal input?
● Check communication between the DSP(IC109) and the CODEC(IC241) as follows:
• Does a PCM signal reach IC109-72pin (ADIN)?
• Does 2MHz reach IC241-14pin CLKIN?
● Check communication between the DSP-G/A(IC101) and the DSP(IC109) as follows:
• Does the channel pulse reach IC109-24,25pin(FSR,FSX)?
• Is a PCM signal output to IC101-23pin (/DPD) synchronizing with CCK1, CDE-X and CDE-Y?
• Is IC109-39pin RESET "H"? Does 2048MHz reach IC109-53pin X2/CLK?
Refer to Schematic Diagram.
Replace the applicable parts.

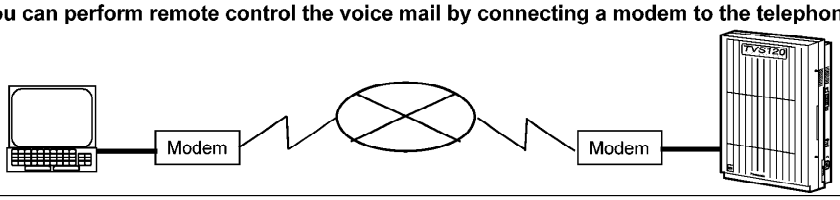
10.11. HOW TO INSTALL A PROGRAM TO HDD

1.You can install a program in the master Hard Disk Drive to slave Hard Disk Drive by using this command.


------The way-------
1.Turn off the power supply, and connect the master HDD and slave HDD to main board by using HDD copy cable (EC1,EC2).
2.Turn on the power supply and input the "SYSD" command by using connected terminal PC. After finished install by indication of the terminal, turn off the power supply.
Please refer to the service manual for details on the master and slave jumper settings.
EC1
EC2
Destination of copy
Original for copy
>
Please Select Your Terminal Type.
1. ASCII TERMINAL
2. VT100
Please Enter the Number := 1
System Administration Top Menu
1. Program
2. System Reports
3. Utility Command
4. System Reset/Clear
Enter the Number := 3
Chose Utility Command
Utility Command(Type 'HELP' for command list.)
$ kme
Enter User ID:KME
Password :=
Enter Password:☐☐☐
All commands are enable.
$ sysd
Please refer to the service manual for command "SYSD".
If you want to update one of program or system guidance or user prompt, please refer to the service manual for command "PCPY" or "GCPY" or "XCPY"

10.12. HOW TO CONNECT THE REMOTE MODEM

1. You can perform remote control the voice mail by connecting a modem to the telephone circuit.



1. Setting the Modem
Setting AT Command:

Q1:All modem responses are disabled
&K0:Disable serial port flow control
S0=:Auto Answer(1 ring)

NOTE:These commands vary with the modem maker. Please check the manual of each modem and set.

2. Connecting KX-TVS120 and the modem
Use a 9pin RS-232C straight cable.

3. Communication speed parameters
Adjust the communication speed/parameters of KX-TVS120 and the PC on the host side (remote).

1) PC on the host side---Set it by following the parameter menu of the communication software (PCPLUS,XTALK, CCT, etc). E.g.) 2400bps, 87data-bit, 1stop-bit, No parity
2) Between KX-TVS120 and modem---When setting the AT commands using the PC as shown above(1), set the same speed/parameters as those of the PC on the host side.
3) KX-TVS120---Following the instructions of the [Program-Hardware Setting-RS-232C Menu] set the same speed/ parameters as for the PC on the host side.

4. Setting speed between modems
Setting the modem speed is usually not needed. However, it is desirable to set the speed according to the Baud Rate which is programmed in KX-TVS120.

NOTE: The AT commands vary with the modem maker. Please check the manual of each modem and set.

● **EMDM COMMAND (External modem setup)**

(1) Function
Used to specify modem commands you want to send to external modem connected with VPS.
(2) Operand
Nothing.
(3) Usage example
You can set up to 5 AT commands and comments (information) for each command.

Modem Command Example

ATE0Q1&D0&S0=1&K0&Q0%C0
E0 :Commands are not echoed.
Q1 : Disable responses to PC
&D0 : Ignore DTR signal
&S0=1 : DSR always ON (auto answer ON)
&K0 : Disables flow control
&Q0 : Select direct asynchronous mode
%C0 : Data compression disable

The modem commands for connecting with VPS vary with the modem maker. Please check the manual of the modem.

```
$ emdm

Current AT Commands for External Modem is as follows.
 No.1 Comment : ZOOM
    Command : AT&D0&K0&Q0\N1%C0Q1S0=1&W0

Please enter command number you want to change.
 If you want to initialize all data, enter 0 :=1
===== Command No.1 =====
Enter Comment(Max:32 Characters) =>TEST
Enter Command(Max:60 Characters) =>ATQ1&K0S0

Current AT Commands for External Modem is as follows.
 No.1 Comment : test
    Command : ATQ1&K0S0

Please enter command number you want to change.
 If you want to initialize all data, enter 0 :=

      To send the AT commands,
       1.Connect Modem and VPS using RS232C Straight Cable
       2.Access System Manager Service
            and press 9 + Command No. during the Top Menu
             Ex.*999 + 91 ( to send Command No.1 )

$
```

Comment

Modem Command

How to send the Modem Command to external modem

Connect the RS-232C straight cable between VPS and modem.
NOTE: You have to turn "PUTD" mode back to "OFF" if you already set the mode to "ON" for trouble shooting.
To send the command, access the System Manager Service, and enter 9 + NO. during the top menu.
For example, *999 + 91 (← VPS sends AT Command No.1).
After sending AT Command, VPS beeps for about 2 sec.

RS-232C CONNECTION WITH KX-TVS120 AND US ROBOTICS MODEM

KX-TVS120: RS-232C MALE PIN NO	MODEM: RS-232C MALE PIN NO
2	2
3	3
5;6	1
20	4

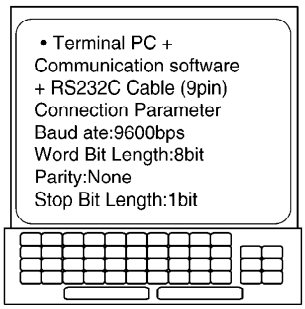
The modems on the list are compatible with KX-TVS120 only using RS-232C straight cable and following "AT" commands. Us Robotics is also compatible using the special connection described above.

LIST OF COMPATIBLE MODEMS FOR KX-TVS120

MODEL	AT COMMANDS	
ACCURA 28.8:33.6 V.34+FAX/HAYES & ZOOM V.34 Model 470	E0	Commands are not echoed
	Q1	Disable responses to PC
	&D0	Ignore DTR signal
	&S0=1	DSR always ON (auto answer ON)
	&k0	Disables flow control
	&Q0	Select direct asynchronous mode
	%C0	Data compression disable
MAXTECH 28.8FAX MODEM	E0	C ommands are not echoed
	Q1	Disable responses to PC
	&D0	Ignore DTR signal
	6S0=1	DRS always ON (auto answer ON)
	Q0	Turn OFF flow control
	N0	Normal data link only
MODEMSURFR 33.6 MOTOROLA	E0	Commands are not echoed
	Q1	Disable responses to PC
	&D0	Ignore DTR signal
	&S0=1	DRS always ON (auto answer ON)
	%C0	Data compression disable
	N0	Normal data link only
	G0	Disable modem to modem flow conrol
	Q0	Disable modem to PC flow control
US ROBOTICS SPORTSTER 22.8 DIP switches position 1,4,8 are ON (down)	E0	Commands are not echoed
	Q1	Disable responses to PC
	&D0	Ignore DTR signal
	&S0=1	DRS always ON (auto answer ON)
	&K0	Data compression disable
	&M0	Normal mode, error control disabled
	&H0	Disable folw control
	S0=1	Answer after 1 ring in AA mode

10.13. HOW TO MAKE A SELF-DIAGNOSIS BY USING MANUFACTURING EXAMINATION MODE

• How to switch to Manufacturing Examination mode.




```
>
Please Select Your Terminal Type.

 1. ASCII TERMINAL
 2. VT100

Please Enter the Number := 1

System Administration Top Menu

 1. Program
 2. System Reports
 3. Utility Command
 4. System Reset/Clear

Enter the Number := 3        <-- Chose Utility Command

Utility Command( Type 'HELP' for command list. )

$ kme                        <-- Enter User ID:KME
Password :=                  <-- Enter Password:␣␣␣
All commands are enable.
$ diag                       <-- Enter Manufacturing
OK 03                            Examination Switch Command
#
```

DIAG (Switch to Self-Diagnosis mode)

Format : DIAG

Function : Switch to Self-Diagnosis mode

Reply : OK 03 : Normal
State of option card installation
(Bit0~1 : Slot1~2 installation
Ex.) Slot1,2 installation : 000011=03h)
NG : No option card is installed.

1. Communication check between CPU and DSP.

DVER 1/A (Communication check between CPU and DSP-IC109)

Format : DVER 1
Unit No. (1~3)

Function : • Indicate the ROM version of DSP.
• Be used to check communication between CPU and DSP.

Reply : OK 0100 : Normal / version.
NG 2 : FIFO communication is abnormal.

2. Communication check of Hard Disk Drive.

HDTS 1 (Communication check between CPU and Hard Disk Drive)

Format : HDTS 1
Drive No. (1: MASTER 2: SLAVE)

Function : • Check the communication between CPU and Hard Disk Drive.

Reply : OK : Normal.
NG 1 : Read Data Impediment.
NG 2 :HDD Controller Impediment.
NG 3 : Sector Impediment.

3. Unit Initialize

UNIN 1 / A (Initialize of Circuit Interface Unit)

Format : UNIN 1 / A
Sorts of circuits (A: Analog SLT / D: Digital)
Unit No. (1~3)

Function : • Be able to record / replay.
• Designate a Slot No. in the first parameter and a used circuit in the second parameter.

Reply : OK : Normal.
NG 2 : FIFO communication is abnormal.

4. SLT DTMF Output Test (Output Command)

1) UNIN 1 / A (Initialize of Circuit Interface Unit: SLT)
2) HOOK 1 / A / 0 (Hooking Control of SLT Interface)

Format : HOOK 1 / A / 0
1 : ON - HOOK 0 : OFF - HOOK
Channel No. (A~B)
Unit No. (1~3)

Function : • At analog-SLT, switch ON / OFF a HOOK bit of I / O port.
• At digital, notify HOOK to the PBX.

Reply : Noting.

5. SLT DTMF Output Test (Output Command)

1) UNIN 1 / A (Initialize of Circuit Interface Unit: SLT)
You don 't need to install the above 1) twice.
DTMF 1 / A / 0 (DTMF output check)

Format : DTMF 1 / A / 0
Sorts of DTMF Tone (1~0, * ,#)
Channel No. (A~B)
Unit No. (1~3)

Function : • Output DTMF tone to the channel designated.

Reply : Nothing.

6. SLT DTMF Output Test (Stop Command)

1) UNIN 1 / A (Initialize of Circuit Interface Unit: SLT)
You don 't need to install the above 1) twice.
DTME 1 / A (DTME output check)

Format : DTME 1 / A
Channel No. (A~B)
Unit No. (1~3)

Function : • Stop DTMF Tone

Reply : OK : Normal.
NG 2 : Receiving Buffer is empty.
NG 3 : FIFO communication is abnormal.

7. DPT communication check

1) UNIN 1 / D (Initialize of Circuit Interface Unit: DPT)
You don 't need to install the above 1) twice.
DPIT 1 (DPT communication check)

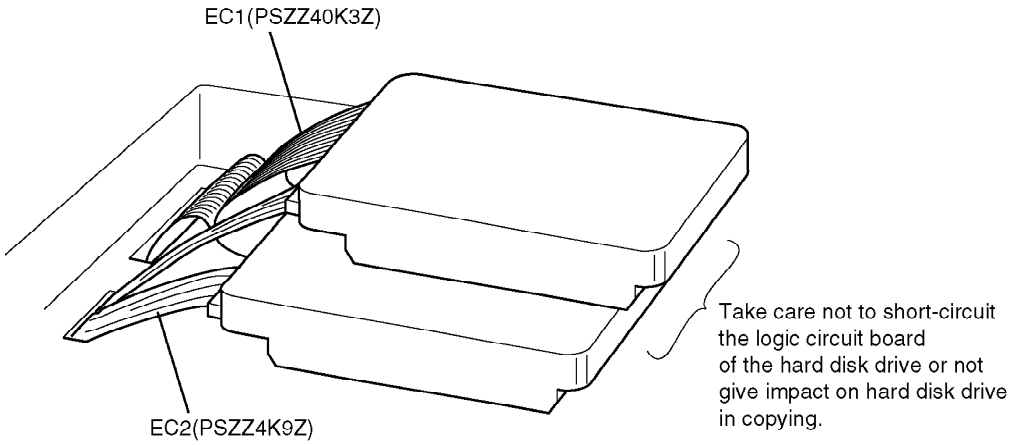
Format : DPIT 1
Unit No. (1~3)

Function : • Start DPT communication

Reply : OK : Normal.
NG 1 : Unable to connect.
NG 2 : Receiving Data is abnormal.

11. HDD INSTALLATION PROCEDURE

11.1. HOW TO USE THE HDD COPY CABLES



Set and connect the unit serving as the copy source to function as the master and the unit serving as the copy destination to function as the slave and, after startup using the master disk, input the copy commands shown below from the terminal and copy the data.

1. To start up with POWER ON Master HDD.

2. Select "1. ASCII TERMINAL" as Terminal Type.

3. Select "3. Utility Command".

4. Input "KME" and password. (PANASONIC)

5. Input command "SYSD" and select option No.0

6. Data copy is complete after 25 minutes.

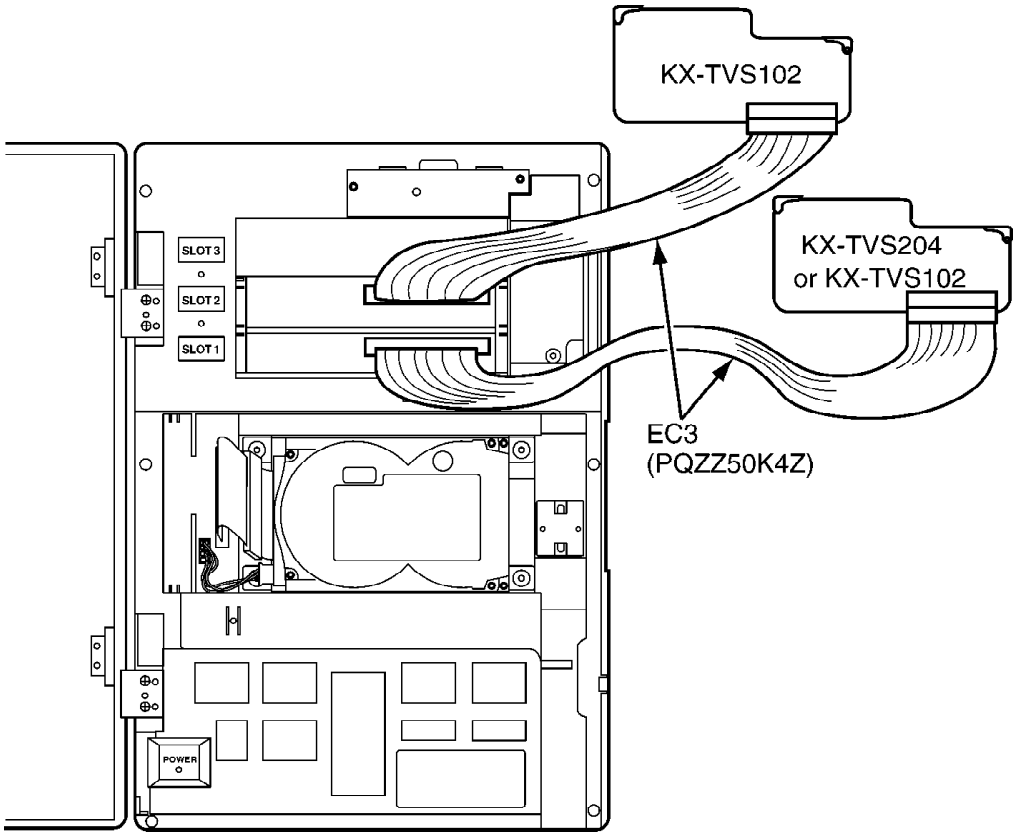
7. Put HDD, HDD cable back, then start up with power on.

8. Installation is complete with Power off --- Power on. Can be used.

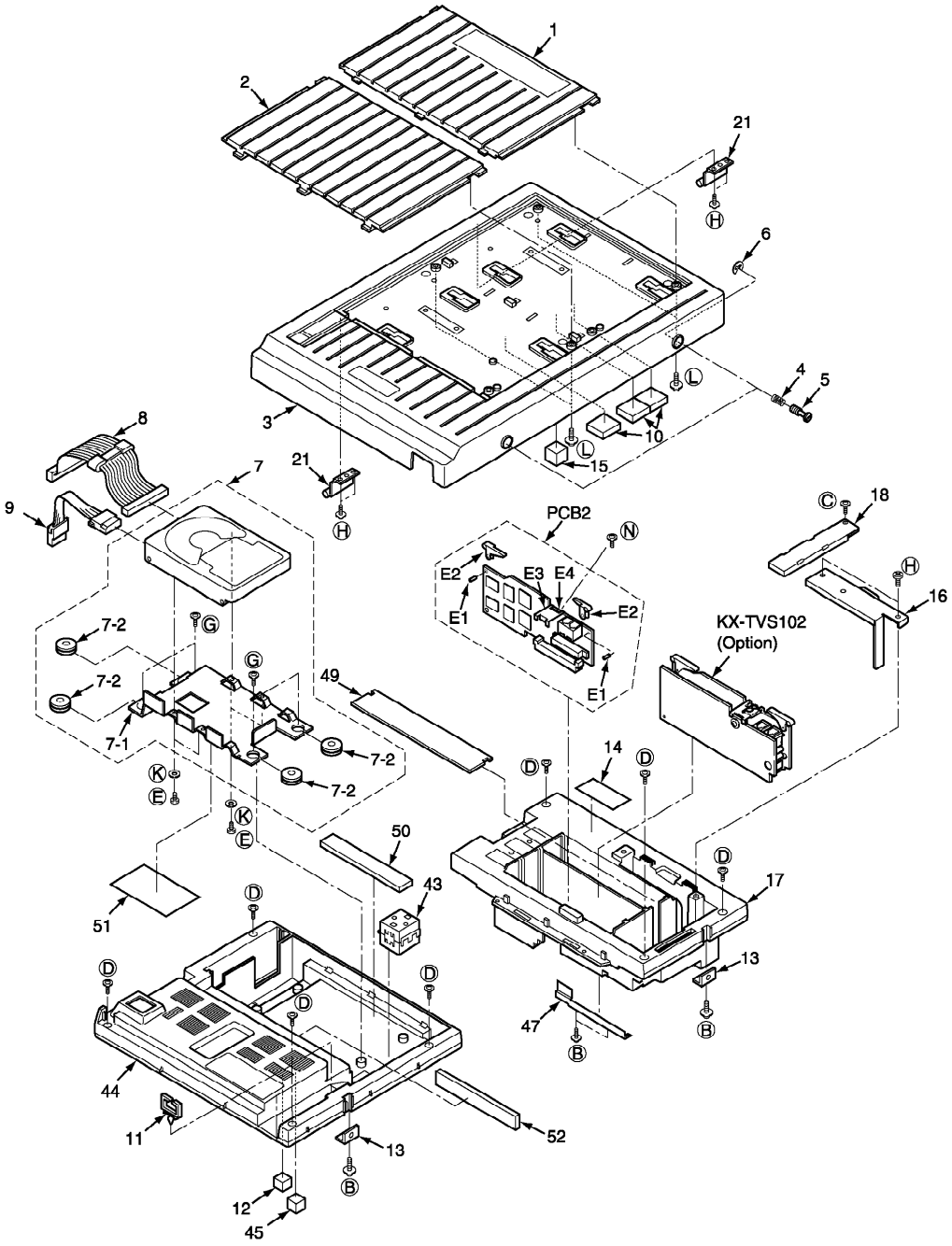
For details on the master and slave jumper settings, refer to Setting the Driver's Jumpers or to the Specifications Manual issued by the hard disk drive manufacturer.

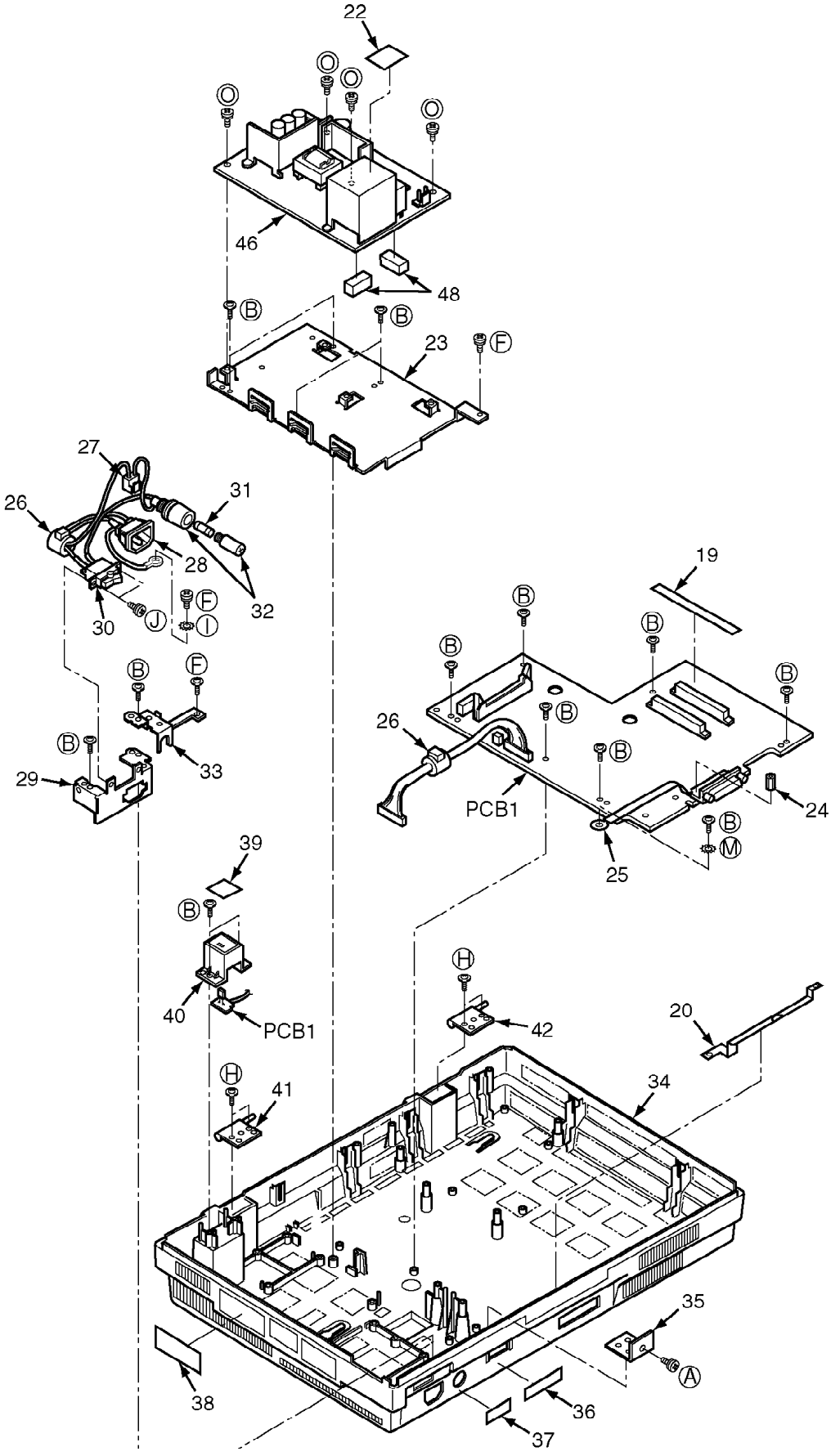
11.2. HOW TO USE THE EXTENSION SLOT CABLES

How to use the expansion slot service cables.
Connect the cables to the expansion slot, pull out TVS102, and check the signal waveforms and voltage value.

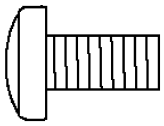
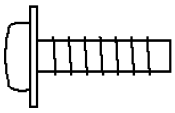
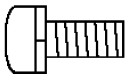
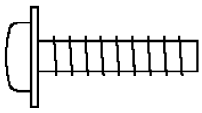
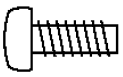
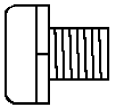
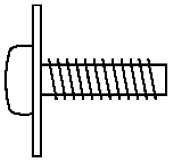
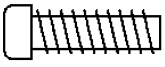
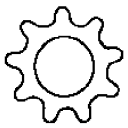


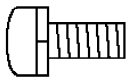
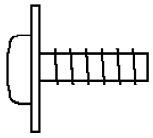
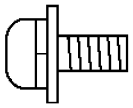
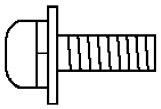
12. CABINET AND ELECTRICAL PARTS LOCATION


1
2
21
Ⓗ
6
4
5
Ⓛ
3
10
Ⓛ
15
8
9
7
21
Ⓗ
PCB2
Ⓝ
E2
E3
E4
E1
E2
E1
Ⓒ
18
Ⓗ
16
KX-TVS102
(Option)
7-2
Ⓖ
7-2
Ⓖ
49
7-1
7-2
7-2
Ⓚ
Ⓔ
Ⓚ
Ⓔ
Ⓓ
14
Ⓓ
50
Ⓓ
17
43
51
Ⓓ
Ⓓ
Ⓓ
Ⓓ
13
47
Ⓑ
Ⓑ
44
11
52
13
Ⓑ
12
45

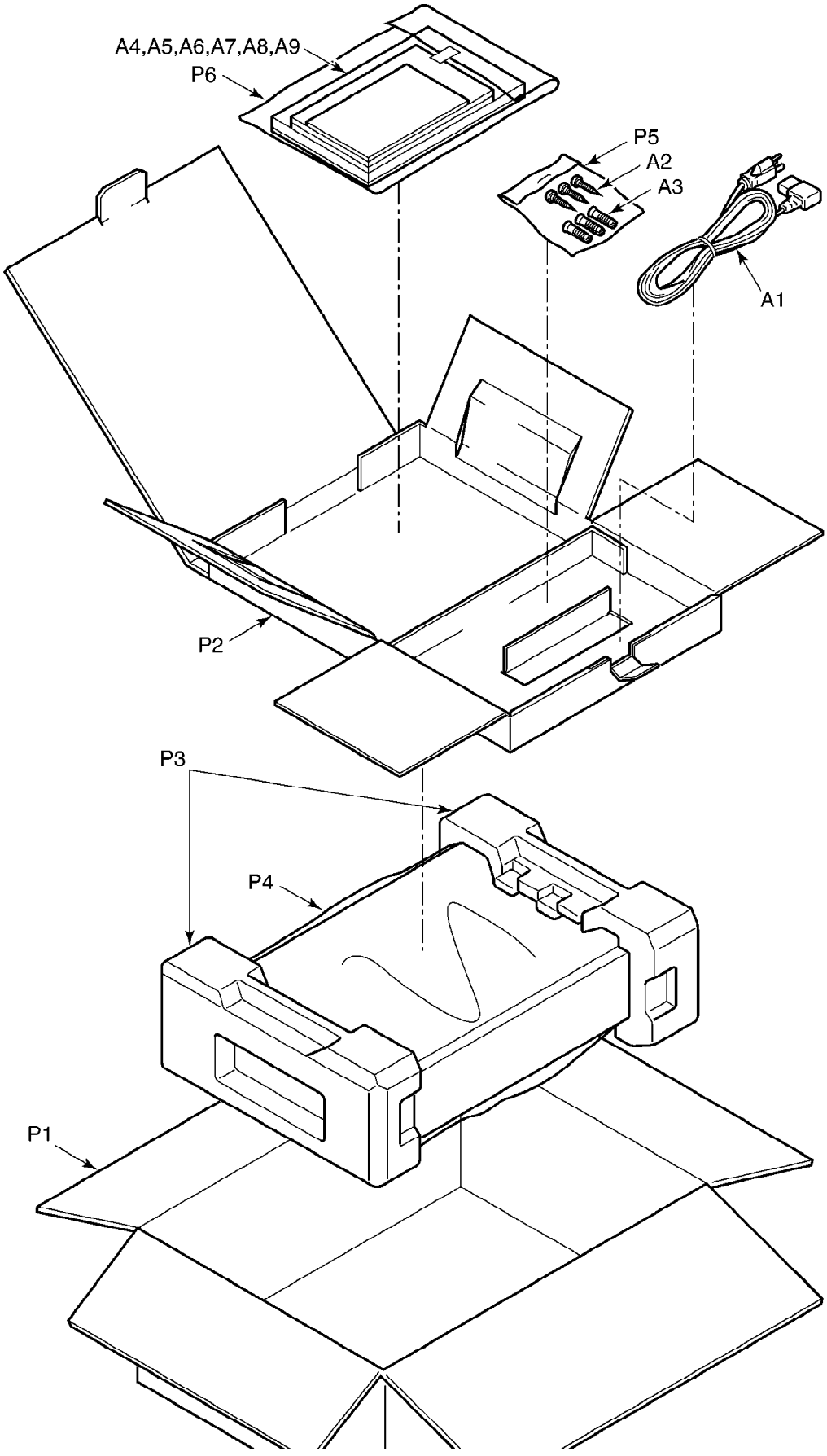

22
46
48
23
27
26
31
28
30
32
29
33
19
26
PCB1
24
25
39
40
PCB1
42
20
41
34
35
38
36
37

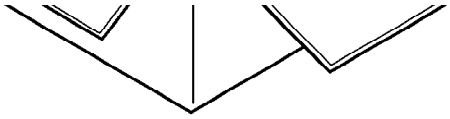
12.1. ACTUAL SIZE OF SCREWS AND WASHER

Ref. No.	Part No.	Figure
Ⓐ	XYM4+EP8BN	
Ⓑ	XTW3+S10P	
Ⓒ	XYN3+F8FN	
Ⓓ	XTW3+S14P	
Ⓔ	XSN6X32+6	
Ⓕ	XYN4+C8	
Ⓖ	PJYC3+MC12	
Ⓗ	XTB3+10GFN	
Ⓘ	XWC4B	

Ⓙ	XYN3+C6	
Ⓚ	XWA35B	
Ⓛ	XTW3+W8F	
Ⓜ	XWC3B	
Ⓝ	XYN3+F6FU	
Ⓞ	XYN3+F8	

13. ACCESSORIES AND PACKING MATERIAL


A4,A5,A6,A7,A8,A9
P6
P5
A2
A3
A1
P2
P3
P4
P1



14. REPLACEMENT PARTS LIST

Note:

1. **RTL (Retention Time Limited)**
   The marking (RTL) indicates that the Retention Time is limited for this item.
   After the discontinuation of this assembly in production, the item will continue to be available for a specific period of time. The retention period of availability depends on the type of assembly and the laws governing parts and product retention. At the end of this period, the assembly will no longer be available.
2. **Important safety notice**
   Components identified by the ⚠ mark indicates special characteristics important for safety. When replacing any of these components, only use specified manufacture's parts.
3. **The S mark means the part is one of some identical parts. For that reason, it may be different from the installed part.**
4. **RESISTORS & CAPACITORS**
   Unless otherwise specified;
   All resistors are in ohms (Ω), k=1000 Ω , M=1000k Ω
   All capacitors are in MICRO FARADS (μ F), p= μ (μ F)
   ***Type & Wattage of Resistor**

Type

ERC:Solid ERD:Carbon PQRD:Carbon	ERX:Metal Film ERG:Metal Oxide ER0:Metal Film	PQ4R:Carbon ERS:Fusible Resistor ERF:Cement Resistor

Wattage

10,16:1/8W	14,25:1/4W	12:1/2W	1:1W	2:2W	3:3W

*Type & Voltage of Capacitor

Type

ECFD:Semi-Conductor ECQS:Styrol PQCUV:Chip ECQMS:Mica	ECCD,ECKD,ECBT,PQCBC:Ceramic ECQE,ECQV,ECQG:Polyester ECEA,ECSZ:Electlytic ECQP:Polypropylene

Voltage

ECQ Type	ECQG ECQV Type	ECSZ Type	Others	
1H:50V 2A:100V 2E:250V 2H:500V	05:50V 1:100V 2:200V	0F:3.15V 1A:10V 1V:35V 0J:6.3V	0J :6.3V 1A :10V 1C :16V 1E,25:25V	1V :35V 50,1H:50V 1J :63V 2A :100V

14.1. CABINET AND ELECTRICAL PARTS

Ref. No.	Part No.	Part Name & Description	Remarks
1	PSKV1025W1	COVER	
2	PQKV10005U1	COVER	
3	PQKE10021L1	FRONT COVER	
4	PSUS1022Z	SPRING	
5	PQHD10011V	SCREW	
6	XUC3VW	RETAINING RING	
7	PSWETVS120M	HEAD DISK DRIVE UNIT ASS'Y (RTL)	
7-1	PSMH1093Z	FRAME, HDD	
7-2	PSHG1094Z	RUBBER PARTS, SPACER	
8	PSJS40P09Z	CONNECTOR, 40P	
9	PSJS04R87Z	CONNECTOR, 4P	
10	PSHG1175	RUBBER	
11	PQHR118Z	CLAMPER	
12	PSHG1111Z	RUBBER PARTS, SPACER	
13	PQMH10008Z	ANGLE	
14	PQQT10918Z	INDICATION LABEL	
15	PSHG1064Z	RUBBER PARTS, SPACER	
16	PSMD1010Z	ANGLE	
17	PQKE10037U1	PARTING PLATE	
18	PSMD1011Z	ANGLE	
19	PSHX1057Z	COVER	
20	PSMH1120Z	MAGNETIC SHIELD PLATE	
21	PQMH10009Z	HINGE	
22	PSQT1308Z	INDICATION LABEL	
23	PSMH1104Z	FRAME, POWER SUPPLY BOARD	
24	PQHE7011Z	NUT	
25	PSWW1001Z	LEAD WIRE	
26	PSLB5D2	FERRITE CORE	S
27	PSJS02R91Z	CONNECTOR, 2P	
28	PQJP3A3Z	AC INLET	⚠
29	PQMH10027Y	CHASSIS	
30	EST15304T	SWITCH, POWER	⚠
31	XBA2C25ND1L	FUSE	⚠
32	PQJV5Z	FUSE HOLDER	⚠
33	PSMH1043Z	ANGLE	
34	PQKM10086F1	CABINET BODY	
35	PQMC10059Y	MAGNETIC SHIELD PLATE	
36	PSQT1314Y	INDICATION LABEL	
37	PSQT1277Y	INDICATION LABEL	
38	PSGT2349Z	NAME PLATE	
39	PQGP10009Z1	PANEL	
40	PQGG10009Z1	GRILLE	
41	PQMH10010Y	HINGE	
42	PQMH10010Z	HINGE	
43	PSLB5F2	FERRITE CORE	
44	PQKF10066U1	INSIDE COVER	
45	PSHG1112Z	RUBBER PARTS, SPACER	
46	PSLP1047Z	POWER SUPPLY BOARD ASS'Y(RTL)	⚠

Ref. No.	Part No.	Part Name & Description	Remarks
47	PSMH1121Z	FG PLATE	
48	PSHG1113Z	RUBBER	
49	PSHR1260Z	COVER, SLOT	
50	PSHG1164Z	RUBBER	
51	PSHG1165Z	SHEET	
52	PSHG1163Z	SPACER	

Note:
Replace a whole power supply block (PSLP1047Z) without replacing individual parts on the board.

14.2. ACCESSORIES AND PACKING MATERIALS

Ref. No.	Part No.	Part Name & Description	Remarks
A1	PSJA1062Z	POWER CORD, AC	⚠ S
A2	PQHE5008Z	MOUNTING BRACKET, SCREW	
A3	PQHE10Z	MOUNTING BRACKET, PLUG	
A4	PQQX10552W	TEMPLATE	
A5	PQQX10970Y	REFERENCE CARD	
A6	PSQW1862Z	LEAFLET, CD-ROM/FCC LEAFLET	
A7	PSQX2719Z	SUBSCRIBER'S GUIDE	
A8	PSQX2721ZCD	INSTLLATION MANUAL SUBSCRIBER'S GUIDE, CD-ROM	
A9	PSQW1863Z	LEAFLET, PROMPT LEAFLET	
P1	PSPK2087Z	PACKING CASE	
P2	PSPN1130Z	ACCESSORY BOX	
P3	PQPN10196Y	CUSHION	
P4	PQPP10022Z	PROECTION COVER (FOR VPS)	
P5	XZBO5X08A03	PROECTION COVER (FOR SCREWS)	
P6	XZB30X40A04	PROECTION COVER (FOR MANUALS)	

14.3. MAIN/LED BOARD PARTS

Ref. No.	Part No.	Part Name & Description	Remarks
PCB1	PSWP1TVS120M	MAIN/LED BOARD ASS'Y (RTL)	
IC301	PSVI68301FGG	IC	
IC302	PQVIPD656109	IC	
IC303	PSVIMT8952BP	IC	
IC304	PFVIMS5148EF	IC	S
IC305	PFVIMS5148EF	IC	S
IC306	PSWITVS120M	IC (ROM)	
IC307	PFVIMS5148EF	IC	S
IC308	PQVIMS6242BG	IC	
IC309	PFVIMS5148EF	IC	S
IC310	PQVIPS520C	IC	
IC311	PQVIDS14C232	IC	
IC312	PQVISN7L245S	IC	S
IC313	PQVISN7L245S	IC	S
IC314	PQVISN7L244S	IC	S
IC315	PQVISN7L244S	IC	S
IC316	PQVISN7L244S	IC	S
IC317	PQVISN7L244S	IC	S
IC318	PQVISN7L245S	IC	S
IC319	PQVISN7L244S	IC	S
IC320	PQVISN7L244S	IC	S
IC321	PQVISN7L244S	IC	S
IC322	PQVISN7L244S	IC	S
		(TRANSISTOR)	
Q301	PQVTDTC143E	TRANSISTOR(SI)	
		(DIODES)	
D300	MA723	DIODE(SI)	
D301	MA742	DIODE(SI)	
D801	LN242RP	DIODE(SI)	
		(BATTERY)	
BAT301	CR23541GUF	LITHIUM BATTERY	
		(CONNECTORS)	
CN301	PQJP40A09Z	CONNECTOR, 40P	
CN302	PQJS50S33Z	CONNECTOR, 50P	
CN303	PQJS50S33Z	CONNECTOR, 50P	
CN305	PSJS12R89Y	CONNECTOR, 12P	
CN306	PQJP2D70Z	CONNECTOR, 2P	
CN307	PQJS25P31Z	SOCKET, 25P	
CN308	PSJP04A46Z	CONNECTOR, 4P	
TM801	PQJS02R48Y	CONNECTOR, 2P	
		(CAPACITORS)	
C3A1	ECUV1H221JCV	220p	S
C3A2	ECUV1H102KBV	0.001	
C3A3	ECUV1H150JCV	15p	S
C3A4	ECUV1H270JCV	27p	S
C3A5	ECUV1H270JCV	27p	S
C3A6	ECUV1H680JCV	68p	S

Ref. No.	Part No.	Part Name & Description	Remarks
C3A7	ECUV1C104ZFV	0.1	
C3A8	ECUV1C104ZFV	0.1	
C3A9	ECUV1C104ZFV	0.1	
C3B0	ECUV1H680JCV	68p	S
C3B1	ECUV1C104ZFV	0.1	
C3B2	ECUV1C104ZFV	0.1	
C3B3	ECUV1C104ZFV	0.1	
C3B4	ECUV1C104ZFV	0.1	
C3B5	ECUV1C104ZFV	0.1	
C3B6	ECUV1H270JCV	27p	S
C3B7	ECUV1H680JCV	68p	S
C3B8	ECUV1H680JCV	68p	
C3B9	ECUV1H680JCV	68p	S
C3C0	ECUV1H221JCV	220p	S
C3C1	ECUV1E104ZFV	0.1	S
C3C2	ECUV1E104ZFV	0.1	S
C3C3	ECUV1E104ZFV	0.1	S
C3C4	ECUV1E104ZFV	0.1	S
C3C5	ECUV1E104ZFV	0.1	S
C3C6	ECUV1E104ZFV	0.1	S
C3C7	ECUV1E104ZFV	0.1	S
C3C8	ECUV1E104ZFV	0.1	S
C3C9	ECUV1C104ZFV	0.1	
C3D0	ECUV1C104ZFV	0.1	
C3D1	ECUV1C104ZFV	0.1	
C3D2	ECUV1C104ZFV	0.1	
C3D3	ECUV1C104ZFV	0.1	
C3D4	ECUV1C104ZFV	0.1	
C3D5	ECUV1C104ZFV	0.1	
C3D6	ECUV1C104ZFV	0.1	
C3D7	ECUV1C104ZFV	0.1	
C3D8	ECUV1C104ZFV	0.1	
C3D9	ECUV1C104ZFV	0.1	
C3E0	ECUV1C104ZFV	0.1	
C3E1	ECUV1C104ZFV	0.1	
C3E2	ECUV1C104ZFV	0.1	
C3E3	ECUV1C104ZFV	0.1	
C301	ECUV1H102KBV	0.001	
C302	ECUV1H102KBV	0.001	
C304	ECEA1EU101	100	S
C305	ERJ3GEY0R00	0(RESISTOR)	
C306	ECUV1H680JCV	68p	
C308	ECUV1H102KBV	0.001	
C309	ECUV1E104ZFV	0.1	S
C310	ECUV1E104ZFV	0.1	S
C311	ECUV1C104ZFV	0.1	
C312	ECUV1C104ZFV	0.1	
C313	ECUV1C104ZFV	0.1	

Ref. No.	Part No.	Part Name & Description	Remarks
C314	ECUV1C104ZFV	0.1	
C315	ECUV1C104ZFV	0.1	
C316	PQCUV1H102J	0.001	S
C317	ECUV1H104ZFV	0.1	S
C318	ECUV1C104ZFV	0.1	
C319	ECUV1H200JCV	20p	S
C320	ECUV1H200JCV	20p	S
C321	ECUV1C104ZFV	0.1	
C322	ECEA1HKS4R7	4.7	
C323	ECEA1EU101	100	S
C324	ECEA1EU101	100	S
C325	ECEA1HKS4R7	4.7	
C326	ECEA1HKS4R7	4.7	
C327	ECEA1HKS4R7	4.7	
C328	ECEA1HKS4R7	4.7	
C329	PQCUV1H5R0CC	5	S
C330	PQCUV1H5R0CC	5	S
C331	ECEA1EU101	100	S
C370	ECEA1EU101	100	S
C371	ECEA1EU101	100	S
C372	ECEA1EU331	330	S
C373	ECEA1EU331	330	S
C374	ECEA1EU101	100	S
C380	ECUV1H560JCV	56p	
C381	ECUV1C104ZFV	0.1	
C382	ECUV1C104ZFV	0.1	
C383	ECUV1H104ZFV	0.1	S
C384	ECUV1H560JCV	56p	
C385	ECUV1H104ZFV	0.1	S
C386	ECUV1H104ZFV	0.1	S
C387	ECUV1H104ZFV	0.1	S
C388	ECUV1H102KBV	0.001	
C389	ECUV1H104ZFV	0.1	S
C390	ECUV1A105ZFV	1	S
C391	ECUV1A105ZFV	1	
C392	ECUV1A105ZFV	1	
C393	ECUV1A105ZFV	1	
C394	ECUV1A105ZFV	1	
C395	ECUV1A105ZFV	1	
C396	ECUV1A105ZFV	1	
C397	ECUV1H221JCV	220p	S
C398	ECUV1C104ZFV	0.1	
C399	ECUV1H221JCV	220p	S
		(CERAMIC FILTERS)	
FIL301	PQVFTU50MT	CERAMIC FILTER	
FIL305	PQVFTU50MT	CERAMIC FILTER	
FIL306	PQVFTU50MT	CERAMIC FILTER	

Ref. No.	Part No.	Part Name & Description	Remarks
		(RESISTORS)	
C305	ERJ3GEY0R00	0	
R3AA	ERJ3GEYJ473	47k	
R3AB	ERJ3GEYJ473	47k	
R3AC	ERJ3GEYJ473	47k	
R3AD	ERJ3GEYJ473	47k	
R3AE	ERJ3GEYJ473	47k	
R3AF	ERJ3GEYJ473	47k	
R3A0	ERJ3GEYJ473	47k	
R3A1	ERJ3GEYJ473	47k	
R3A2	ERJ3GEYJ473	47k	
R3A3	ERJ3GEYJ473	47k	
R3A4	ERJ3GEYJ473	47k	
R3A5	ERJ3GEYJ473	47k	
R3A6	ERJ3GEYJ473	47k	
R3A7	ERJ3GEYJ473	47k	
R3A8	ERJ3GEYJ473	47k	
R3A9	ERJ3GEYJ473	47k	
R3B0	PQ4R10XJ103	10k	
R3B1	PQ4R10XJ103	10k	
R3B2	PQ4R10XJ103	10k	
R3B3	PQ4R10XJ103	10k	
R3B4	PQ4R10XJ103	10k	
R3B5	PQ4R10XJ103	10k	
R3B6	PQ4R10XJ103	10k	
R3B7	PQ4R10XJ103	10k	
R3C0	PQ4R10XJ472	4.7k	
R3C1	PQ4R10XJ472	4.7k	
R3C2	PQ4R10XJ472	4.7k	
R3C3	PQ4R10XJ472	4.7k	
R3D0	ERJ3GEYJ330	33	
R3D1	ERJ3GEYJ330	33	
R3D2	ERJ3GEYJ330	33	
R3D3	ERJ3GEYJ330	33	
R3D4	ERJ3GEYJ330	33	
R3D5	ERJ3GEYJ330	33	
R3D6	ERJ3GEYJ330	33	
R3D7	ERJ3GEYJ330	33	
R3D8	ERJ3GEYJ330	33	
R3D9	ERJ3GEYJ330	33	
R3E0	ERJ3GEYJ330	33	
R3E1	ERJ3GEYJ330	33	
R3E2	ERJ3GEYJ330	33	
R3E3	ERJ3GEYJ330	33	
R3E4	ERJ3GEYJ330	33	
R3E5	ERJ3GEYJ330	33	
R3E6	ERJ3GEYJ330	33	
R3E7	ERJ3GEYJ330	33	
R3E8	ERJ3GEYJ330	33	
R3E9	ERJ3GEYJ330	33	

Ref. No.	Part No.	Part Name & Description	Remarks
R3F0	ERJ3GEYJ330	33	
R3F1	ERJ3GEYJ330	33	
R3F2	ERJ3GEYJ330	33	
R3F3	ERJ3GEYJ101	100	
R3F4	ERJ3GEYJ101	100	
R3F5	ERJ3GEYJ330	33	
R3F6	ERJ3GEYJ330	33	
R3F7	ERJ3GEYJ101	100	
R3F8	ERJ3GEYJ101	100	
R3F9	ERJ3GEYJ101	100	
R3G0	ERJ3GEYJ101	100	
R3G1	ERJ3GEYJ101	100	
R3G2	ERJ3GEYJ101	100	
R3G3	ERJ3GEYJ101	100	
R3G4	ERJ3GEYJ101	100	
R3G5	ERJ3GEYJ101	100	
R3G6	ERJ3GEYJ101	100	
R3G7	ERJ3GEYJ101	100	
R3G8	ERJ3GEYJ101	100	
R3G9	ERJ3GEYJ101	100	
R3H0	ERJ3GEYJ101	100	
R3H1	ERJ3GEYJ101	100	
R3H2	ERJ3GEYJ101	100	
R3H3	ERJ3GEYJ101	100	
R3H4	ERJ3GEYJ101	100	
R3H5	ERJ3GEYJ101	100	
R3H6	ERJ3GEYJ103	10k	
R3H7	ERJ3GEYJ103	10k	
R3H8	ERJ3GEYJ103	10k	
R3H9	ERJ3GEYJ103	10k	
R3J0	ERJ3GEYJ103	10k	
R3J1	ERJ3GEYJ103	10k	
R3J2	PQ4R10XJ103	10k	
R3J3	PQ4R10XJ103	10k	
R3J4	PQ4R10XJ103	10k	
R3J5	PQ4R10XJ103	10k	
R3J6	PQ4R10XJ103	10k	
R3J7	PQ4R10XJ103	10k	
R3J8	PQ4R10XJ103	10k	
R3J9	ERJ3GEYJ103	10k	
R3K0	ERJ3GEYJ103	10k	
R3K1	ERJ3GEYJ103	10k	
R3K2	ERJ3GEYJ103	10k	
R3K3	ERJ3GEYJ103	10k	
R3K4	ERJ3GEYJ103	10k	
R3K5	ERJ3GEYJ103	10k	
R3K6	ERJ3GEYJ103	10k	
R3K7	ERJ3GEYJ103	10k	
R3K8	ERJ3GEYJ103	10k	

Ref. No.	Part No.	Part Name & Description	Remarks
R3K9	ERJ3GEYJ103	10k	
R3L0	ERJ3GEYJ103	10k	
R3L1	ERJ3GEYJ103	10k	
R3L2	ERJ3GEYJ103	10k	
R3L3	ERJ3GEYJ103	10k	
R3L4	ERJ3GEYJ103	10k	
R3L5	PQ4R10XJ152	1.5k	
R3L6	ERJ3GEY0R00	0	
R3L9	ERJ3GEYJ330	33	
R3M0	ERJ3GEYJ330	33	
R3M1	ERJ3GEYJ330	33	
R3N0	ERJ3GEYJ103	10k	
R3N1	ERJ3GEYJ103	10k	
R3N2	ERJ3GEYJ103	10k	
R3N3	ERJ3GEYJ103	10k	
R3N4	ERJ3GEYJ103	10k	
R3N5	ERJ3GEYJ103	10k	
R3N6	ERJ3GEYJ103	10k	
R3N7	ERJ3GEYJ103	10k	
R3N8	ERJ3GEYJ103	10k	
R3N9	ERJ3GEYJ103	10k	
R3P0	ERJ3GEY0R00	0	
R3P1	ERJ3GEY0R00	0	
R3P2	ERJ3GEY0R00	0	
R3P3	ERJ3GEY0R00	0	
R3P4	ERJ3GEY0R00	0	
R3P5	ERJ3GEY0R00	0	
R3P6	ERJ3GEY0R00	0	
R3P7	ERJ3GEY0R00	0	
R3P8	ERJ3GEY0R00	0	
R3P9	ERJ3GEY0R00	0	
R3S4	ERJ3GEYJ330	33	
R3S5	ERJ3GEYJ330	33	
R3S6	ERJ3GEYJ330	33	
R3S7	ERJ3GEYJ330	33	
R3S8	ERJ3GEYJ330	33	
R3S9	ERJ3GEYJ330	33	
R3T1	ERJ3GEYJ820	82	
R3T2	ERJ3GEYJ820	82	
R3T3	ERJ3GEYJ820	82	
R3T5	ERJ3GEYJ330	33	
R3T6	ERJ3GEYJ330	33	
R3T7	ERJ3GEYJ330	33	
R3T8	ERJ3GEYJ330	33	
R3T9	ERJ3GEYJ330	33	
R3U0	ERJ3GEYJ330	33	
R3U2	ERJ3GEYJ330	33	

Ref. No.	Part No.	Part Name & Description	Remarks
R3U3	ERJ3GEY0R00	0	
R3U6	ERJ3GEYJ330	33	
R3U7	ERJ3GEYJ330	33	
R3U8	ERJ3GEYJ330	33	
R3U9	ERJ3GEY0R00	0	
R3W1	ERJ3GEYJ330	33	
R3W2	ERJ3GEYJ473	47k	
R3W3	ERJ3GEYJ101	100	
R3W5	ERJ3GEYJ330	33	
R3W6	ERJ3GEYJ330	33	
R3W7	ERJ3GEYJ330	33	
R3W9	ERJ3GEY0R00	0	
R3X0	ERJ3GEY0R00	0	
R3X1	ERJ3GEY0R00	0	
R3X2	ERJ3GEY0R00	0	
R3X3	ERJ3GEY0R00	0	
R3X4	ERJ3GEY0R00	0	
R3X5	ERJ3GEY0R00	0	
R3X6	ERJ3GEY0R00	0	
R3X7	ERJ3GEY0R00	0	
R3Y1	ERJ3GEYJ472	4.7k	
R301	ERJ3GEYJ330	33	
R302	ERJ3GEYJ330	33	
R303	PQ4R10XJ472	4.7k	
R304	ERJ3GEYJ472	4.7k	
R305	ERJ3GEYJ472	4.7k	
R306	ERJ3GEYJ103	10k	
R307	ERJ3GEYJ472	4.7k	
R308	ERJ3GEYJ472	4.7k	
R309	ERJ3GEYJ472	4.7k	
R310	ERJ3GEYJ101	100	
R311	ERJ3GEY0R00	0	
R312	ERJ3GEYJ101	100	
R313	ERJ3GEYJ330	33	
R314	ERJ3GEYJ330	33	
R315	ERJ3GEYJ330	33	
R316	ERJ3GEYJ330	33	
R317	ERJ3GEYJ330	33	
R318	ERJ3GEYJ330	33	
R319	ERJ3GEYJ330	33	
R320	PQ4R10XJ472	4.7k	
R321	ERJ3GEY0R00	0	
R323	ERJ3GEYJ470	47	
R324	ERJ3GEYJ330	33	
R326	ERJ3GEYJ560	56	
R327	PQ4R10XJ821	820	
R329	PQ4R10XJ820	82	

Ref. No.	Part No.	Part Name & Description	Remarks
R330	ERJ3GEYJ221	220	
R331	ERJ3GEYJ473	47k	
R332	ERJ3GEYJ473	47k	
R333	PQ4R10XJ473	47k	
R334	ERJ3GEYJ472	4.7k	
R336	PQ4R10XJ473	47k	
R337	PQ4R10XJ473	47k	
R338	PQ4R10XJ473	47k	
R339	PQ4R10XJ473	47k	
R340	ERJ3GEY0R00	0	
R341	ERJ3GEY0R00	0	
R342	ERJ3GEYJ103	10k	
R343	ERJ3GEY0R00	0	
R344	ERJ3GEY0R00	0	
R345	ERJ3GEY0R00	0	
R346	ERJ3GEY0R00	0	
R347	ERJ3GEY0R00	0	
R348	ERJ3GEY0R00	0	
R349	ERJ3GEY0R00	0	
R350	ERJ3GEY0R00	0	
R351	ERJ3GEY0R00	0	
R352	ERJ3GEY0R00	0	
R353	ERJ3GEY0R00	0	
R354	ERJ3GEY0R00	0	
R355	ERJ3GEY0R00	0	
R356	ERJ3GEY0R00	0	
R357	ERJ3GEY0R00	0	
R358	ERJ3GEY0R00	0	
R359	ERJ3GEY0R00	0	
R360	ERJ3GEYJ184	180k	
R362	ERJ3GEYJ330	33	
R363	ERJ3GEYJ101	100	
R364	ERJ3GEYJ101	100	
R365	ERJ3GEYJ101	100	
R366	ERJ3GEYJ101	100	
R367	ERJ3GEYJ101	100	
R368	ERJ3GEYJ101	100	
R369	ERJ3GEYJ101	100	
R370	PQ4R10XJ103	10k	
R372	PQ4R10XJ473	47k	
R373	ERJ3GEYJ473	47k	
R374	ERJ3GEYJ473	47k	
R375	PQ4R10XJ473	47k	
R376	PQ4R10XJ103	10k	
R377	ERJ3GEY0R00	0	
R378	ERJ3GEY0R00	0	
R379	ERJ3GEY0R00	0	
R380	ERJ3GEY0R00	0	
R381	ERJ3GEY0R00	0	

Ref. No.	Part No.	Part Name & Description	Remarks
R382	ERJ3GEY0R00	0	
R383	ERJ3GEY0R00	0	
R384	ERJ3GEY0R00	0	
R385	ERJ3GEY0R00	0	
R386	ERJ3GEY0R00	0	
R387	ERJ3GEY0R00	0	
R388	ERJ3GEY0R00	0	
R389	ERJ3GEY0R00	0	
R390	ERJ3GEY0R00	0	
R391	ERJ3GEY0R00	0	
R392	ERJ3GEY0R00	0	
R393	ERJ3GEY0R00	0	
R394	ERJ3GEY0R00	0	
R394	ERJ3GEY0R00	0	
R395	ERJ3GEY0R00	0	
R396	ERJ3GEY0R00	0	
R397	ERJ3GEY0R00	0	
R398	ERJ3GEY0R00	0	
R399	ERJ3GEY0R00	0	
R801	PQ4R10XJ221	220	
		(COILS)	
R3Q0	PQLQR1RM601	COIL	
R3Q1	PQLQR1RM601	COIL	
R3Q2	PQLQR1RM601	COIL	
R3Q3	PQLQR1RM601	COIL	
R3Q4	PQLQR1RM601	COIL	
R3Q5	PQLQR1RM601	COIL	
R3Q6	PQLQR1RM601	COIL	
R3Q7	PQLQR1RM601	COIL	
R3Q8	PQLQR1RM601	COIL	
R3Q9	PQLQR1RM601	COIL	
R3R0	PQLQR1RM601	COIL	
R3R1	PQLQR1RM601	COIL	
R3R2	PQLQR1RM601	COIL	
R3R3	PQLQR1RM601	COIL	
R3R4	PQLQR1RM601	COIL	
R3R5	PQLQR1RM601	COIL	
R3V4	PQLQR1RM601	COIL	
R3W0	PQLQR1RM601	COIL	
R3X8	PQLQR1RM601	COIL	
R3X9	PQLQR1RM601	COIL	
R325	PQLQR1RS121	COIL	
		(SWITCH)	
SW301	PQSR10A101Z	R0TARY SWITCH	
		(CRYSTAL OSCILLATORS)	
X300	PQVCL3276N6Z	CRYSTAL OSCILLATOR	
X301	PSVCCR3276B2	CRYSTAL OSCILLATOR	

14.4. DPT INTERFACE CARD PARTS

Ref. No.	Part No.	Part Name & Description	Remarks
PCB2	PSWP2TVS120M	DPT INTERFACE CARD ASS'Y(RTL)	
		(ICs)	
IC101A	PQVIPD656214	IC	
IC101B	PQVIPD656214	IC	
IC102	PQVISN7L244S	IC	S
IC103	PQVISN7L244S	IC	S
IC104	PQVISN7L245S	IC	S
IC105	PQVISN7L241M	IC	S
IC106A	PQVISN7L126A	IC	S
IC106B	PQVISN7L126A	IC	S
IC107	PSVITC7S08FU	IC	
IC108	C0JBAE000087	IC	
IC109A	PSVI8C060BPJ	IC	
IC109B	PSVI8C060BPJ	IC	
IC109C	PSVI8C060BPJ	IC	
IC109D	PSVI8C060BPJ	IC	
IC261A	PQVINJM319V	IC	
IC261B	PQVINJM319V	IC	
		(TRANSISTORS)	
Q100A	PQVTDTC143E	TRANSISTOR(SI)	
Q100B	PQVTDTC143E	TRANSISTOR(SI)	
Q261A	2SB1218A	TRANSISTOR(SI) (or 2SA1576Q)	
Q261B	2SB1218A	TRANSISTOR(SI) (or 2SA1576Q)	
Q262A	2SB1218A	TRANSISTOR(SI) (or 2SA1576Q)	
Q262B	2SB1218A	TRANSISTOR(SI) (or 2SA1576Q)	
		(CONNECTORS & JACK)	
CN101	PQJP50S33Z	CONNECTOR, 50P	
CN103	PSJJ2T004Z	JACK, TEL	
		(CAPACITORS)	
C100	ECUV1H102KBV	0.001	
C101A	ECUV1H102KBV	0.001	
C101B	ECUV1H102KBV	0.001	
C102A	ECUV1H120JCV	12p	
C102B	ECUV1H120JCV	12p	
C103A	ECUV1H120JCV	12p	
C103B	ECUV1H120JCV	12p	
C104A	ECUV1C104ZFV	0.1	
C104B	ECUV1C104ZFV	0.1	
C105A	ECUV1C104ZFV	0.1	
C105B	ECUV1C104ZFV	0.1	
C106A	ECUV1H101JCV	100p	
C106B	ECUV1H101JCV	100p	
C107A	ECUV1H101JCV	100p	
C107B	ECUV1H101JCV	100p	
C108A	ECUV1H102KBV	0.001	
C108B	ECUV1H102KBV	0.001	

Ref. No.	Part No.	Part Name & Description	Remarks
C109A	ECUV1H102KBV	0.001	
C109B	ECUV1H102KBV	0.001	
C110A	ECUV1H102KBV	0.001	
C110B	ECUV1H102KBV	0.001	
C111A	ECUV1H102KBV	0.001	
C111B	ECUV1H102KBV	0.001	
C112A	ECUV1H102KBV	0.001	
C112B	ECUV1H102KBV	0.001	
C113A	ECUV1H102KBV	0.001	
C113B	ECUV1H102KBV	0.001	
C114A	ECUV1H102KBV	0.001	
C114B	ECUV1H102KBV	0.001	
C114C	ECUV1H102KBV	0.001	
C114D	ECUV1H102KBV	0.001	
C115A	ECUV1C104ZFV	0.1	
C115B	ECUV1C104ZFV	0.1	
C115C	ECUV1C104ZFV	0.1	
C115D	ECUV1C104ZFV	0.1	
C116A	PQCUV1H223KB	0.022	
C116B	PQCUV1H223KB	0.022	
C116C	PQCUV1H223KB	0.022	
C116D	PQCUV1H223KB	0.022	
C117A	ECUV1C391JCV	390p	
C117B	ECUV1C391JCV	390p	S
C117C	ECUV1C391JCV	390p	S
C117D	ECUV1C391JCV	390p	S
C118A	ECUV1C104ZFV	0.1	
C118B	ECUV1C104ZFV	0.1	
C118C	ECUV1C104ZFV	0.1	
C118D	ECUV1C104ZFV	0.1	
C119A	PQCUV1C105ZF	1	
C119B	PQCUV1C105ZF	1	
C119C	PQCUV1C105ZF	1	
C119D	PQCUV1C105ZF	1	
C120A	ECUV1C104ZFV	0.1	
C120B	ECUV1C104ZFV	0.1	
C120C	ECUV1C104ZFV	0.1	
C120D	ECUV1C104ZFV	0.1	
C121A	ECUV1C104ZFV	0.1	
C121B	ECUV1C104ZFV	0.1	
C121C	ECUV1C104ZFV	0.1	
C121D	ECUV1C104ZFV	0.1	
C122E	ECUV1H220JCV	22p	
C123E	ECUV1H100DCV	10p	
C130	ECEA1AU221	220	S
C131	ECUV1C104ZFV	0.1	
C132	ECUV1C104ZFV	0.1	
C133	ECUV1C104ZFV	0.1	
C134	ECUV1C104ZFV	0.1	
C135	ECUV1C104ZFV	0.1	
C136	ECUV1C104ZFV	0.1	
C137	ECUV1C104ZFV	0.1	
C138	ECUV1C104ZFV	0.1	
C139	ECUV1C104ZFV	0.1	

Ref. No.	Part No.	Part Name & Description	Remarks
C140	ECUV1C104ZFV	0.1	
C141	ECUV1C104ZFV	0.1	
C142	ECUV1C104ZFV	0.1	
C143	ECUV1C104ZFV	0.1	
C144	ECUV1C104ZFV	0.1	
C145	ECUV1C104ZFV	0.1	
C146	ECUV1C104ZFV	0.1	
C147	ECEA1AU470	47	S
C230A	ECUV1C104ZFV	0.1	
C230B	ECUV1C104ZFV	0.1	
C233A	ECUV1C104ZFV	0.1	
C233B	ECUV1C104ZFV	0.1	
C234A	ECUV1C104ZFV	0.1	
C234B	ECUV1C104ZFV	0.1	
C261A	ECEV1HA010	1	
C261B	ECEV1HA010	1	
C262A	ECEV1HA010	1	
C262B	ECEV1HA010	1	
C263A	ECUV1H680JCV	68p	
C263B	ECUV1H680JCV	68p	
C264A	ECUV1H680JCV	68p	
C264B	ECUV1H680JCV	68p	
C265A	ECUV1H101JCV	100p	
C265B	ECUV1H101JCV	100p	
C266A	ECUV1H101JCV	100p	
C266B	ECUV1H101JCV	100p	
C267A	ECUV1H470JCV	47p	
C267B	ECUV1H470JCV	47p	
C268A	ECUV1H470JCV	47p	
C268B	ECUV1H470JCV	47p	
C269A	PQCUV1H223KB	0.022	
C272A	ECUV1C104ZFV	0.1	
C272B	ECUV1C104ZFV	0.1	
C291A	ECEA1HN2R2S	2.2	S
C291B	ECEA1HN2R2S	2.2	S
		(COILS)	
L110	PQLQR1RS121	COIL	
L112A	PQLQR1RS121	COIL	
L112B	PQLQR1RS121	COIL	
L291A	PQLQR1LT	COIL	
L291B	PQLQR1LT	COIL	
L292A	PQLQR1LT	COIL	
L292B	PQLQR1LT	COIL	
		(RESISTORS)	
L111	ERJ3GEY0R00	0	
R100A	ERJ3GEYJ330	33	
R100B	ERJ3GEYJ330	33	
R102	ERJ3GEYJ330	33	
R105A	ERJ3GEYJ473	47k	
R105B	ERJ3GEYJ473	47k	
R107A	ERJ3GEY0R00	0	
R107B	ERJ3GEY0R00	0	

Ref. No.	Part No.	Part Name & Description	Remarks
R108A	ERJ3GEYJ471	470	
R108B	ERJ3GEYJ471	470	
R110A	ERJ3GEYJ330	33	
R110B	ERJ3GEYJ330	33	
R111A	ERJ3GEYJ330	33	
R111B	ERJ3GEYJ330	33	
R112A	ERJ3GEYJ330	33	
R112B	ERJ3GEYJ330	33	
R113A	ERJ3GEYJ330	33	
R113B	ERJ3GEYJ330	33	
R114A	ERJ3GEYJ330	33	
R114B	ERJ3GEYJ330	33	
R115A	ERJ3GEYJ473	47k	
R115B	ERJ3GEYJ473	47k	
R115C	ERJ3GEYJ473	47k	
R115D	ERJ3GEYJ473	47k	
R116A	ERJ3GEYJ272	2.7k	
R116B	ERJ3GEYJ272	2.7k	
R116C	ERJ3GEYJ272	2.7k	
R116D	ERJ3GEYJ272	2.7k	
R117A	ERJ3GEYJ473	47k	
R117B	ERJ3GEYJ473	47k	
R117C	ERJ3GEYJ473	47k	
R117D	ERJ3GEYJ473	47k	
R118A	ERJ3GEYJ473	47k	
R118B	ERJ3GEYJ473	47k	
R118C	ERJ3GEYJ473	47k	
R118D	ERJ3GEYJ473	47k	
R119A	ERJ3GEYJ473	47k	
R119B	ERJ3GEYJ473	47k	
R119C	ERJ3GEYJ473	47k	
R119D	ERJ3GEYJ473	47k	
R120A	ERJ3GEYJ473	47k	
R120B	ERJ3GEYJ473	47k	
R120C	ERJ3GEYJ473	47k	
R120D	ERJ3GEYJ473	47k	
R121A	ERJ3GEYJ473	47k	
R121B	ERJ3GEYJ473	47k	
R121C	ERJ3GEYJ473	47k	
R121D	ERJ3GEYJ473	47k	
R122A	ERJ3GEYJ473	47k	
R122B	ERJ3GEYJ473	47k	
R122C	ERJ3GEYJ473	47k	
R122D	ERJ3GEYJ473	47k	
R123A	ERJ3GEYJ473	47k	
R123B	ERJ3GEYJ473	47k	
R123C	ERJ3GEYJ473	47k	
R123D	ERJ3GEYJ473	47k	
R124A	ERJ3GEYJ473	47k	
R124B	ERJ3GEYJ473	47k	
R124C	ERJ3GEYJ473	47k	
R124D	ERJ3GEYJ473	47k	
R133	ERJ3GEYJ103	10k	
R134	ERJ3GEYJ103	10k	

Ref. No.	Part No.	Part Name & Description	Remarks
R135	ERJ3GEYJ103	10k	
R136	ERJ3GEYJ103	10k	
R137	ERJ3GEYJ680	68	
R138	ERJ3GEYJ470	47	
R141A	ERJ3GEYJ473	47k	
R141B	ERJ3GEYJ473	47k	
R142A	ERJ3GEYJ473	47k	
R142B	ERJ3GEYJ473	47k	
R142C	ERJ3GEYJ473	47k	
R142D	ERJ3GEYJ473	47k	
R143A	ERJ3GEYJ103	10k	
R143B	ERJ3GEYJ103	10k	
R144A	ERJ3GEYJ103	10k	
R144B	ERJ3GEYJ103	10k	
R145A	ERJ3GEYJ103	10k	
R145B	ERJ3GEYJ103	10k	
R146A	ERJ3GEYJ103	10k	
R146B	ERJ3GEYJ103	10k	
R147A	ERJ3GEYJ103	10k	
R147B	ERJ3GEYJ103	10k	
R148A	ERJ3GEYJ103	10k	
R148B	ERJ3GEYJ103	10k	
R149A	ERJ3GEYJ103	10k	
R149B	ERJ3GEYJ103	10k	
R150B	ERJ3GEYJ103	10k	
R261A	ERJ3GEYJ330	33	
R261B	ERJ3GEYJ330	33	
R262A	ERJ3GEYJ330	33	
R262B	ERJ3GEYJ330	33	
R263A	ERJ3GEYJ472	4.7k	
R263B	ERJ3GEYJ472	4.7k	
R264A	ERJ3GEYJ472	4.7k	
R264B	ERJ3GEYJ472	4.7k	
R265A	ERJ3GEYJ472	4.7k	
R265B	ERJ3GEYJ472	4.7k	
R266A	ERJ3GEYJ472	4.7k	
R266B	ERJ3GEYJ472	4.7k	
R267A	ERJ3GEYJ472	4.7k	
R267B	ERJ3GEYJ472	4.7k	
R268A	ERJ3GEYJ472	4.7k	
R268B	ERJ3GEYJ472	4.7k	
R269A	ERJ3GEYJ472	4.7k	
R269B	ERJ3GEYJ472	4.7k	
R270A	ERJ3GEYJ472	4.7k	
R270B	ERJ3GEYJ472	4.7k	
R271A	ERJ3GEYJ472	4.7k	
R271B	ERJ3GEYJ472	4.7k	
R272A	ERJ3GEYJ472	4.7k	
R272B	ERJ3GEYJ472	4.7k	
R273A	ERJ3GEYJ821	820	
R273B	ERJ3GEYJ821	820	
R274A	PQ4R10XF8201	8.2k	S
R275A	PQ4R10XF1201	1.2k	S
R276A	ERJ3GEYJ330	33	

Ref. No.	Part No.	Part Name & Description	Remarks
R276B	ERJ3GEYJ330	33	
R277A	ERJ3GEYJ330	33	
R277B	ERJ3GEYJ330	33	
R291A	PQRQ1VJ821	820	
R291B	PQRQ1VJ821	820	
		(TRANSFORMERS)	
T291A	PSLT9Z7A	TRANSFORMER	
T291B	PSLT9Z7A	TRANSFORMER	
		(CRYSTAL OSCILLATORS)	
X100A	PSVCCS1638G5	CRYSTAL OSCILLATOR	
X100B	PSVCCS1638G5	CRYSTAL OSCILLATOR	
		(VARISTORS)	
ZR291A	ERZC07DK820	VARISTOR	
ZR291B	ERZC07DK820	VARISTOR	
ZR292A	ERZC07DK820	VARISTOR	
ZR292B	ERZC07DK820	VARISTOR	
		(OTHERS)	
E1	PQDF996Z	SHAFT	
E2	PSHR1104Z	GUIDE	
E3	PQMH10151Z	ANGLE	
E4	PQMH10152Z	LEAF SPRING	

14.5. FIXTURES AND TOOLS

Ref. No.	Part No.	Part Name & Description	Remarks
EC1	PSZZ40K3Z	EXTENTION CORD, 40P (for HDD)	
EC2	PSZZ4K9Z	EXTENTION CORD, 4P (for HDD)	
EC3	PQZZ50K4Z	EXTENTION CORD, 50P (for KX-TVS102,KX-TVS204)	

Notes:
Extension cords are useful for serving. (They make serving easy.)

15. FUNCTIONAL BLOCK DIAGRAM(KX-TVS102)(OPTION)

15.1. KX-TVS102 (DSP/CO CARD)(OPTION)

15.1.1. DSP CARD (KX-TVS102)(OPTION)

DSP block is loaded with DSP (IC109) installed with a 1.3k word RAM and 32k word outside the fixed program ROM (IC107/IC108).
This DSP interfaces CODEC, connected with a SLT interface on a CO block and transforms

voice region signals D/A, A/D, and DPT line.
Each DSP disposes a digital voice region data for each channel described below. Mutual transformation, voice region digital data (64kBPS : 8bit/125us) and ADPCM data (32kBPS : 4 bit/ 125us), are executed. To detect a certain tone (for example DTMF tone or call progress tone) by analyzing input PCM data and to output a certain tone (for example DTMF tone or BEEP tone) as PCM data.
Timing Control on the DSP block is controlled by the system controller (IC101). System controller includes DPT interface, ADPCM compressed voice data transfer control between DSP and system memory, FIFO logic and parallel I/O port to control the SLT circuit line.
DSP receives commands from the host CPU through FIFO (IC101), then works based on the command.
This DSP execution program is stored in the external high speed ROM (IC107/IC108).
The DPT interface logic works to input and output the information data (D channel data) received and sent with the PBX through DPT with a HDLC controller (IC303) on a CPU block. It distributes voice region data (B1,B2 channel data) received and sent by the PBX through a DPT to each DSP(IC109A, IC109B).
The Parallel I/O port, used for SLT interface on the CO block taking status and Hook control, is controlled by the CPU.

SPECIFICATION OF THE DSP CARD

BLOCK	SPECIFICATIONS	DESCRIPTIONS
HOST I/F	50-pin Connector	Signals × 38, +5V × 2, -5V × 2, GND × 8
CO I/F	30-pin Connector	
DSP LSI (IC109)	PQVIMP58C002	Running frequency : 57.344MHz (14.336MIPS)
	Internal RAM	1312 word × 16 (for Program/Data memory)
	Internal ROM	20kword × 16 (not used)
	Serial Port	using DPT digital voice data in/out
	CODEC I/F	using SLT analog voice data in/out
DSP ROM (IC107/IC108)	64kByte (IC107/IC108)	access time : 35nsec

BLOCK	SPECIFICATIONS	DESCRIPTIONS
SLAVE CONTROLLER (IC101)	FIFO	To communicate between Host CPU and DSP
	Parallel I/O Port	bit IA-3 : not used IA-2 : CPU-A detect when 0 IA-1 : not used IA-0 : BELL-A detect when 0
		OA-1 : not used OA-0 : HOOK-A control (0: off-hook)
		IB-3 : not used IB-2 : CPU-B detect when 0 IB-1 : not used IB-0 : BELL-B detect when 0
		OB-1 : not used OB-0 : HOOK-B control (0: off-hook)
		OX-3 : not used OX-2 : not used OX-1 : loop test enable when 0 OX-0 : not used
	Serial Voice Port	for ADPCM Voice Data Transfer Control between DSP ar System Memory
	DPT interface	DPT Frame Formatter and Transceiver

15.1.2. CO CARD (KX-TVS102)(OPTION)

A port in the CO block is a hybrid component and is constructed to add an SLT interface with loop start style to the DPT transceiver.
It is intended to detect the arrival of signals (BELL), to catch circuits (DC loop enable), and to generate a dial pulse by loop on/off and 2-line ~ 4-line transformation (Balance-Network) as a basic function. The 4-line analog data is transformed to digital data by CODEC, then is interfaced with the DSP block.
The DPT transceiver includes the transceiver by transistor (Q261/Q262) and receiver by converter (IC261) and interfaces with PBX through the Pulse Trans (T291).

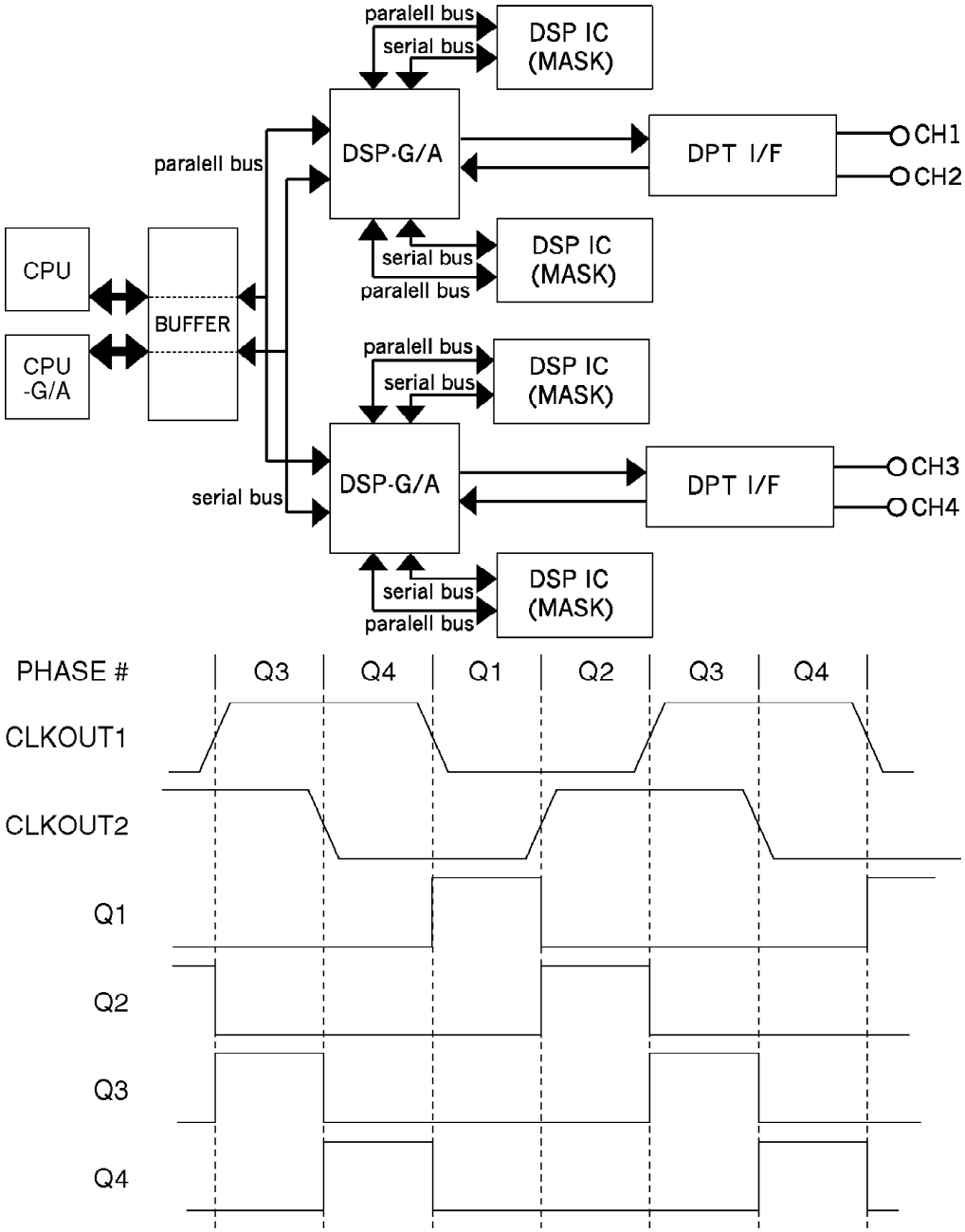
SPECIFICATIONS OF THE CO CARD

<table>
<tr><th>BLOCK</th><th>SPECIFICATIONS</th><th>DESCRIPTIONS</th></tr>
<tr><td>DSP I/F</td><td>30-pin Connector</td><td></td></tr>
<tr><td>CO I/F</td><td>4 pin Modular × 2</td><td>Port-A : DPT/SLT Hybrid I/F
Port-B : SLT I/F</td></tr>
<tr><td>T-R I/F</td><td>BELL Detect</td><td>To Detect the following Bell Signal
Voltage : min 40 Vrms (Frequency : 25 Hz)
The H/W only detects the level/frequency.
The bell cadence should be checked by software algorithm.</td></tr>
<tr><td></td><td>DIAL PULSE Control</td><td>The hardware logic only controls the loop ON/OFF.
Pulse Dialing Cadence is controlled by S/W
Dialing Rate : 10 or 20 PPS
Break to Make Ratio : 60 %
Interdigit Interval : Typical 800 ms</td></tr>
<tr><td></td><td>DTMF TONE Dialing</td><td>DTMF tone is generated by DSP LSI, and DSP sends the DTMF tone to CODEC or D-PITS.
-Tone Level : High Group : -9 dbm
Low Group : -11 dbm
Twist 2 dbm
Harmonics Level: -7 dbm
-Digit Layout : Refer to following Table
High Group [Hz]
<table><tr><td></td><td></td><td>1209</td><td>1336</td><td>1477</td><td>1633</td></tr><tr><td>Low Group</td><td>697</td><td>1</td><td>2</td><td>3</td><td>A</td></tr><tr><td>[Hz]</td><td>770</td><td>4</td><td>5</td><td>6</td><td>B</td></tr><tr><td></td><td>852</td><td>7</td><td>8</td><td>9</td><td>C</td></tr><tr><td></td><td>941</td><td>*</td><td>0</td><td>#</td><td>D</td></tr></table>-Frequency Tolerance : max +/- 1.5%
-Duration : 80 msec
-Interdigit Interval : 100 msec</td></tr>
</table>

16. CIRCUIT OPERATIONS(KX-TVS102)(OPTION)

16.1. DSP CARD (KX-TVS102)

16.1.1. OVERVIEW OF THE DSP CARD(OPTION)



The function of the DSP Card is integrated in the Slave Controller (IC101) and DSP (IC109). These LSI devices include the functions mentioned below.

Slave Controller

- FIFO to communicate between Microprocessor and DSP.
- Voice Port Interface to transfer ADPCM data between system memory and DSP.
- DPT interface to receive and send digital data by DPT protocol.
- Line interface control I/O port to detect BELL, off-hook control, etc.

DSP (IC109)

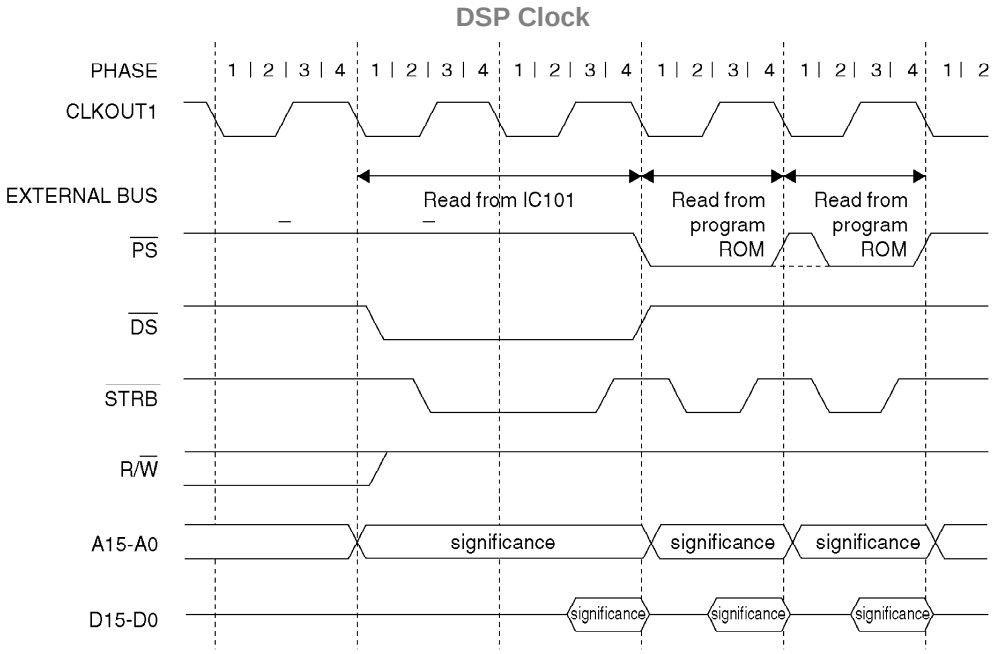
- Compression/extension of voice data by ADPCM algorithm.
- To detect and generate DTMF.
- To detect and generate TONE.
- Detection of VOX (no-sound) condition. (To detect the condition of completed conversation.)
- Automatic gain adjustment of recording level.

16.1.2. CPU CARD INTERFACE

Refer to section 1-10. Expansion Bus.

16.1.3. DSP CLOCK

4.096MHz provided from the CPU card is input to the DSP (IC109 - 53pin) as a basic clock. This clock is input to the PLL inside DSP. PLL generates 14.336MHz (PLLCLK) from this clock. PLLCLK is divided into four inside and generates CLKOUT1 and CLKOUT2. Figure 4-22 is standing of CLKOUT1 and indicates the third phase (Q3) is about to begin. Hereafter, phase no. Q1 - Q4 explains the bus operation.



16.1.4. PARALLEL DSP PORT

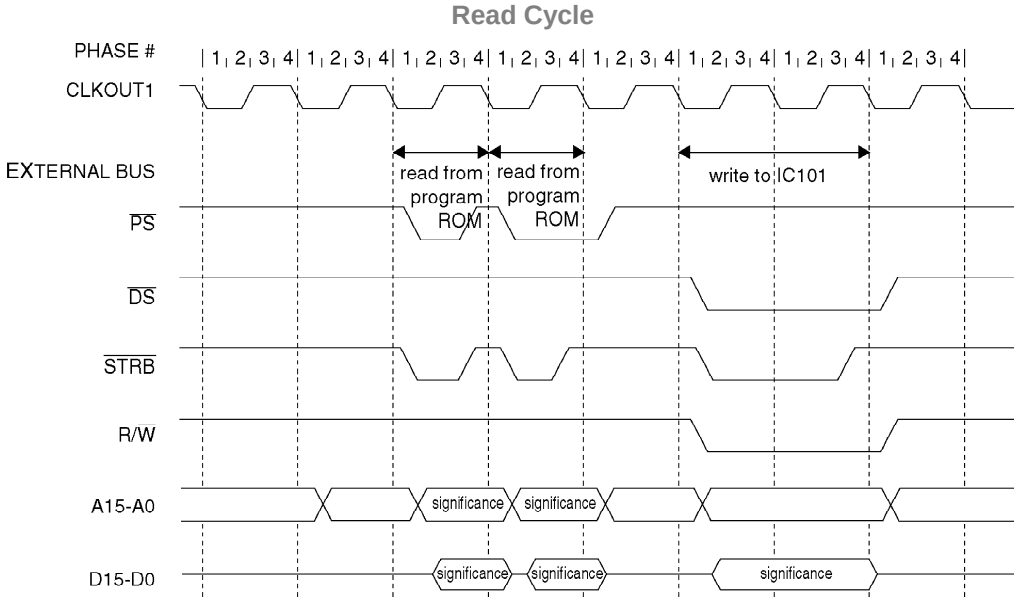
DSP installs control signals mentioned below to interface with Program ROM or IC101 inside register.

- 16bit parallel data bus (A15 - A0)
- 16bit parallel data bus (D15 - D0)
- Chip select (PS, DS)
- Timing Control (STRB, R/WN)

(1) External read out cycle
The following are phenomena generated with the external read out cycle.

1. **In the first phase (Q1), DSP starts driving address bus, and makes either PS or DS low level. To indicate the external memory's read out, R/W signal becomes high level.**
2. **At the beginning of the second phase (Q2), STRB signal indicating the effectiveness of the address bus output, and is used to generate a read enable signal with the R/W signal.**
3. **At the end of the third phase (Q3), data is taken in.**
4. **At the beginning of the fourth phase (Q4), the STRB signal is cancelled. PS, or DS signal and address bus are of no effect, and ends the external read out cycle.**

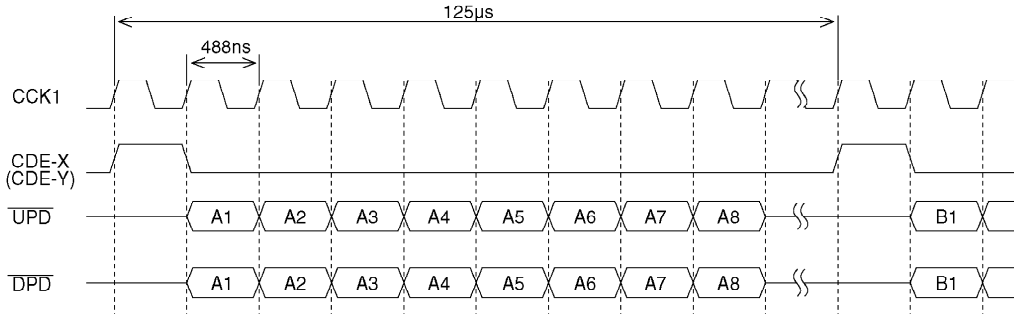
Control signal PS, DS, STRB and R/W are generated only when the external memory location has gained access to. PS is asserted only when Program ROM (IC107/IC108) has gained access. DS is asserted only when the internal register of IC101 has gained access.



(2) External write in cycle
The following are phenomena generated with the external write in cycle.

1. **In the first phase (Q1), DSP starts driving address bus, and makes DS active low. The R/W signal becomes low level for writing in external memory.**
2. **At the beginning of the second phase (Q2), the STRB signal indicates the effectiveness of the address bus output, and is used to generate read a enable signal with the R/W signal.**
3. **At the beginning of the second phase (Q3), data bus becomes active.**
4. **At the beginning of the fourth phase (Q4), the STRB signal is canceled. The Processor makes the address bus and DS signal invalid, and ends access of the external write in cycle.**

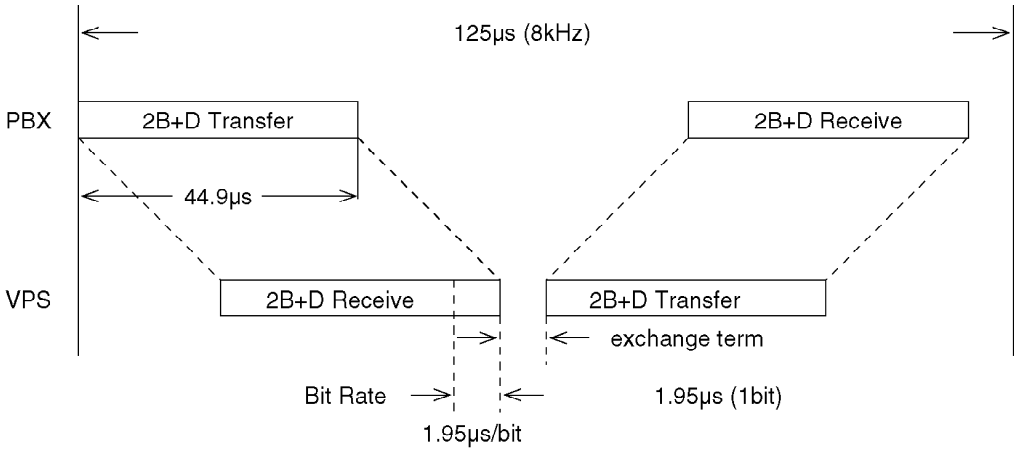
Write Cycle



16.1.5. DSP SERIAL PORT

**DSP serial port is used with the interface for the DPT B channel (Digital Voice Data).
This port is connects IC101 with CCK1, UPD, DPD, CDE-X (IC109A) and CDE-Y (IC109B) signals. CCK1 is a 2.048MHz's serial shift in/out clock. UPD is 8bit PCM formatted voice data output from DSP. It is sent out to the PBX through DPT interface logic internal IC101. DPD is DSP input of PCM formatted voice data received from the PBX. CDE-X (CDE-Y) is an 8 KHz frame pulse input to enable to send or receive effective data of a serial port.
Serial Port Transfer Timing is shown in Timing 4-24.**

DSP Serial Port



16.1.6. DSP CODEC PORT

The DSP Codec Port is input and output from a Single line telephone interface. It is used for interface with a codec converting analog voice data to digital data. DSP uses four interface lines (CLK, ADIN, DIGS and DIGL), then communicates Codec. These signals are connected with Codec (IC 241) on a CO card through CN102.

1.024MHz's CLKA (CLKB) output from the DSP is used as a sampling clock for DAC/ADC internal codec.

ADIN is a serial voice data input to DSP. (Bit rate = 1.024MHz) DIGLA/DIGSA (DIGLB/DIGSB) is 2 bit voice data output from DSP. (Bit rate = 512 KHz)

Input and output timing of Codec Port is shown in Timing 4-25.

DSP Codec Port

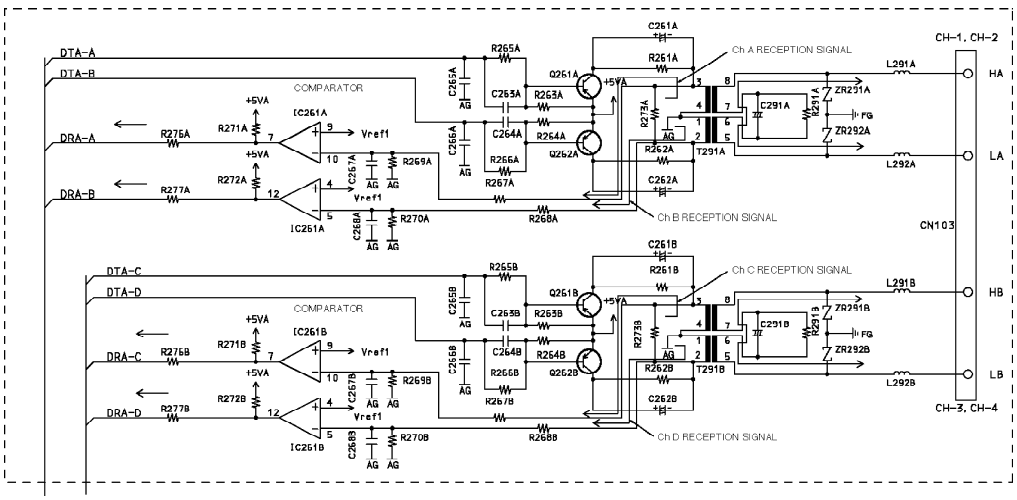
S1	S2	S3	S4	S5	MA1	MA2	MA3	HK	D0	D1	B17	B16	B15	B14	B13	B12	B11	B10	B27	B26	B25	B24	B23	B22	B21	B20	PRY
5					3				2		8								8								1

Function	CN102 pin No.	Description
BELL Detection	9 (BELLA) 5 (BELLB)	These Signals respond to the ring signal from the single line telephone interface.
CPC Detection	7 (CDETA) 3 (CDETB)	These signals indicate temporary disconnection of the single line telephone interface.
Hook Control	12 (PULSA) 8 (PULSB)	These signals control the Hook condition of the single li telephone interface. If it is low, the telephone line is in th OFF-Hook condition. If it is High, it is in the ON-Hook condition.
Loop Back Control	11 (LOOP)	This signal allows loop back testing of the analog voice data for diagnostic. If it is low, it is in test mode. In norm operation, LOOP is held in High.
Reserved	10 (RURSA) 6 (RURSB)	These signals are not used.

16.1.8. DPT DIGITAL INTERFACE

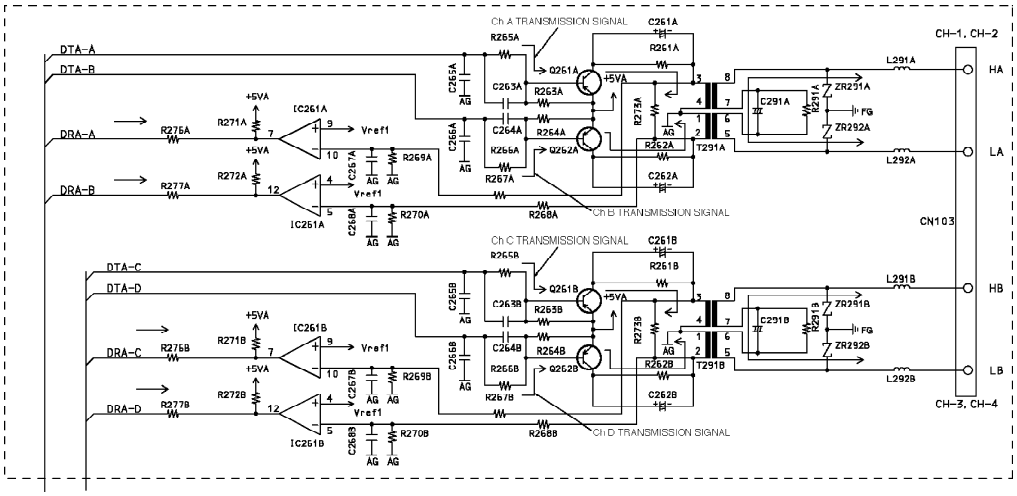
DPT digital interface is provided with IC101. DPT interface built-in IC101 extracts effective data (2B + D) from a receiving DPT data stream, transfers D channel receiving data to voice port, and B channel receiving data (PCM Voice Data) to DSP. Sending out DPT data stream formed with D channel sending out data received from Voice Port and B channel sending out data received from DSP, is output to the CO card.
DPT interface is a digital interface, line bit rate : 512kBPS's, 2 line time share data format. Its communication format is 2B+D (B:64kBPS, D:16kBPS) and executes ping-pong communication every 8kHz (125us).
Data format B channel is 64kBPS u/A PCM format and D channel is 16kBPS HDLC format.

DPT Data Transfer



Bit allotment of the DPITS frame is described below. S(1 - 5) is a zero pattern of 5 bits and is used as hardware to synchronize receiving and sending data with PLL.MA (1 - 3) is a 3-bit zero pattern data against AM1 symbolization and is used to detect the head of effective data. HK sends out an installed value inside the HK port. D(0 - 1) is 2 bit/frame HDLC data channel. B1 (7 - 0), B2 (7 - 0) are received and sent out in an 8-bit PCM data by MSB first individually.

DPT Frame Format

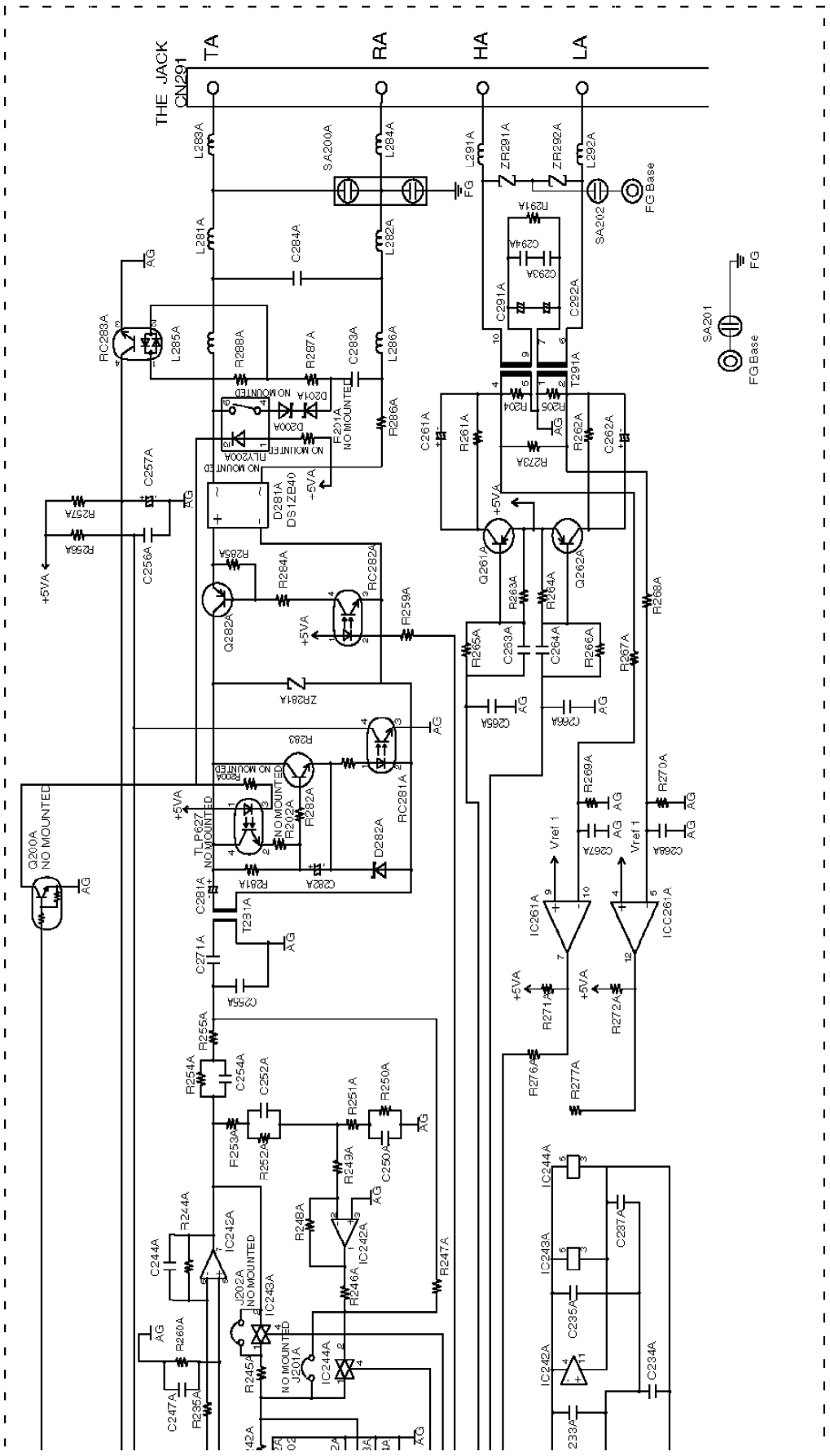


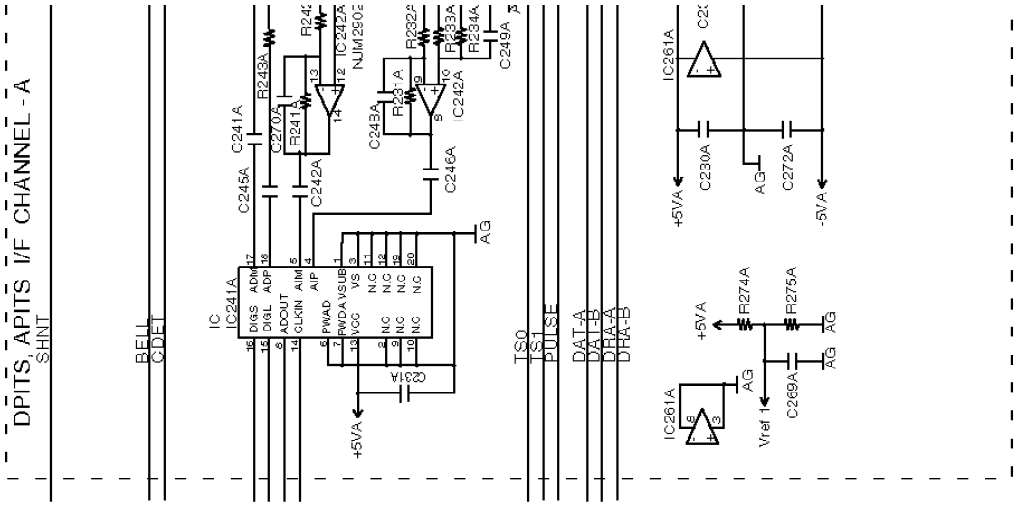
16.2. CO CARD (KX-TVS102)(OPTION)

16.2.1. OVERVIEW OF THE CO CARD

The following figure shows function block diagram of the CO Card.

Functional Block Diagram of CO Card


THE JACK CN291
TA
RA
HA
LA
SA200A
SA201
SA202
FG
FG Base
L288A
L284A
L291A
ZR291A
ZR292A
L292A
L281A
L282A
C284A
R291A
C294A
C293A
C291A
C292A
T291A
RC283A
L285A
R288A
R287A
C283A
L286A
D201A NO MOUNTED
R286A
C261A
R261A
R262A
C262A
R273A
R205
R204
C257A
R257A
R256A
C256A
D281A DS1ZB40
-5VA
+5VA
AG
Q261A
Q262A
R263A
R264A
R268A
Q282A
RC282A
F259A
R265A
C263A
C264A
R266A
R267A
C265A
C266A
ZR281A
R283
RC281A
R282A
R202A
D282A
C282A
R281A
C281A
T231A
C271A
C255A
Q200A NO MOUNTED
TLP627 NO MOUNTED
R269A
R270A
C267A
C268A
Vref 1
IC261A
ICC261A
R271A
R272A
R276A
R277A
R255A
R254A
C254A
C252A
R253A
R252A
R251A
R250A
C250A
R249A
R248A
IC242A
R247A
R246A
C244A
R244A
R260A
C247A
R235A
J202A NO MOUNTED
IC243A
J201A NO MOUNTED
IC244A
R245A
IC244A
IC243A
IC242A
C297A
C295A
C234A
238A

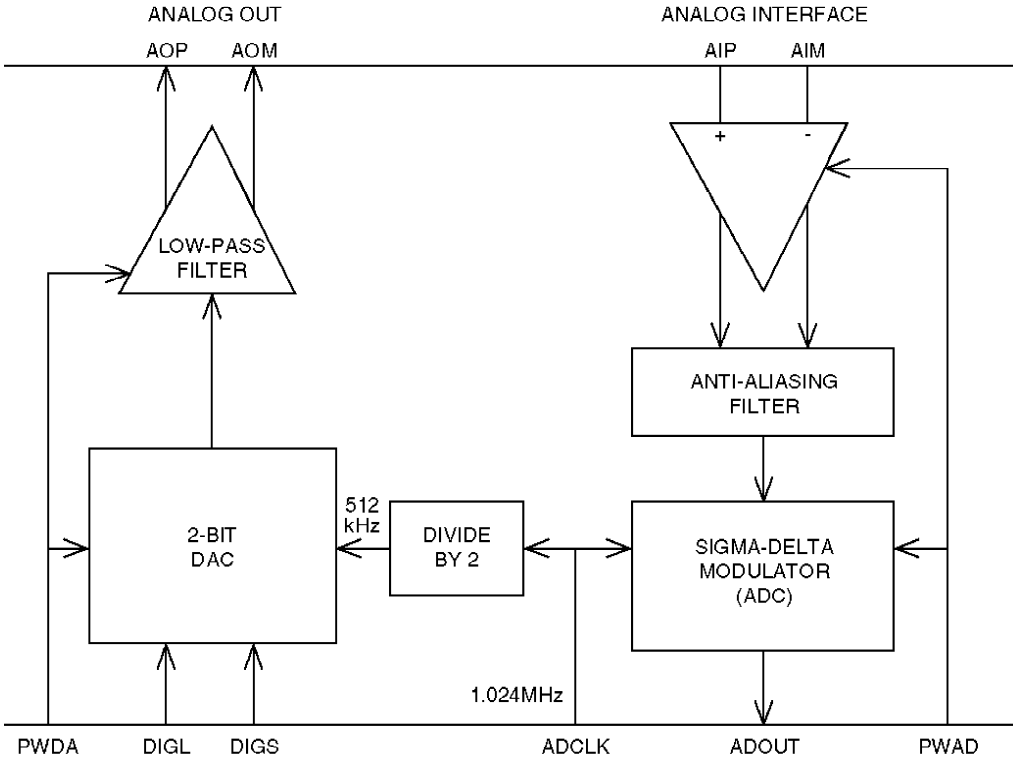


The CO Card possesses 2 channels, SLT (Single line Telephone) interface and 1 channel DPT line interface.
The SLT interface includes Codec, Amplifier, 4W - 2W Converter, Transformer CPC Detector, Hook Control, Bridge and Bell detector.
The DPT interface includes Receiver, Transceiver and Transformer.

16.2.2. CODEC (IC241)

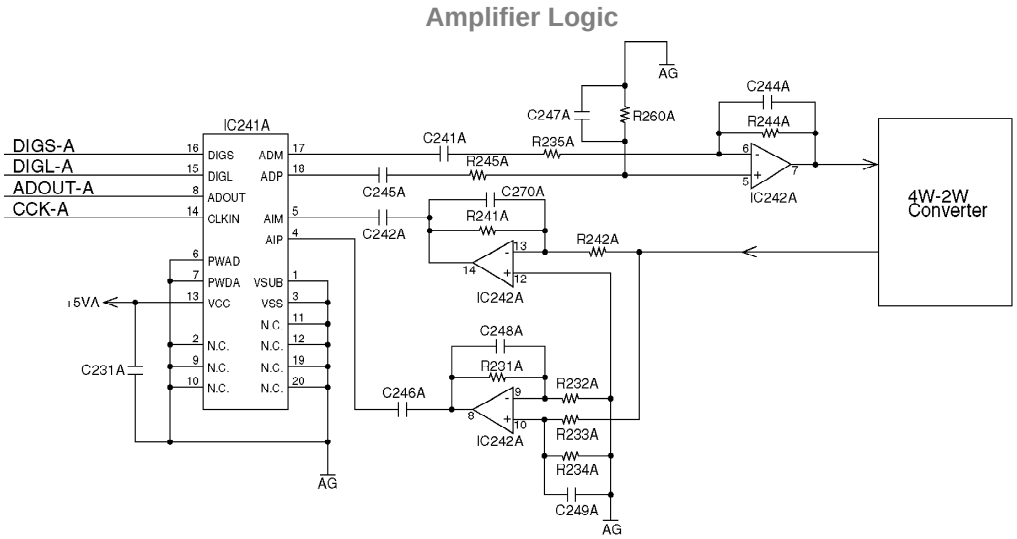
The Codec provides a voice-band ADC and DAC. The Codec communicates with the DSP using a 4 interface line (DIGS, DIGL, ADOUT and CLKIN). The DAC logic can synchronously operate in full duplex with ADC.
The following figure shows the internal function block.

Codec Internal Block Diagram



16.2.3. AMPLIFIER (IC242)

This logic amplifies the voice band analog level.



The data flow is shown as the follows.

•Transmit Voice Data

IC241 - 17 (ADM out) → C241 → R235 → IC242 - 6 → IC242 - 7 → 4w - 2w Converter.

IC241 - 18 (ADP out) → C245 → R243 → IC242 - 5

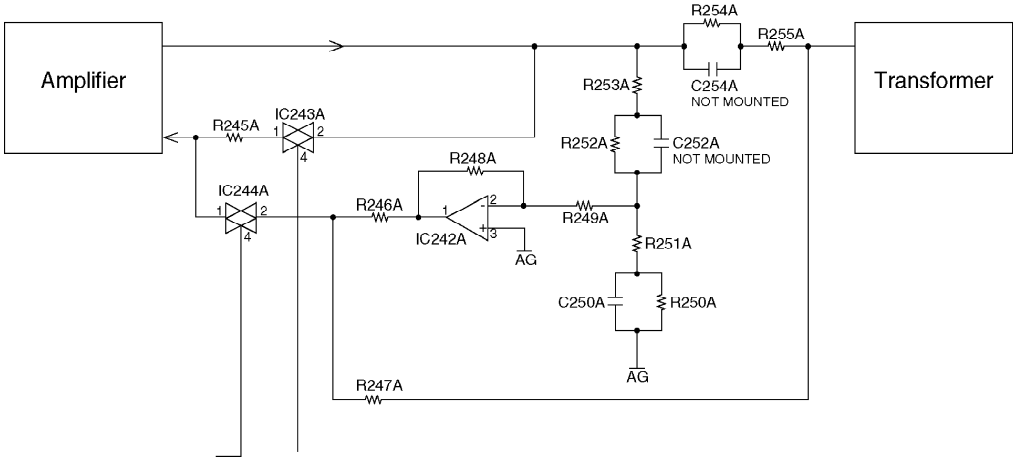
•Receive Voice Data

4w - 2w Converter → R242 → C242 - 13 → IC242 - 14 → C242 → IC241 - 5 (AIMin)

→ R233 → C242 - 10 → IC242 - 8 → C246 → IC241 - 4 (AIPin)

16.2.4. 4W-2W CONVERTER

4W-2W Converter Logic



This logic converts 4 line analog signal to 2 line analog signal.

The data flow is the followings.

•Transmit Voice data

Amplifier → R254 → R255 → Transformer (Transmit data)

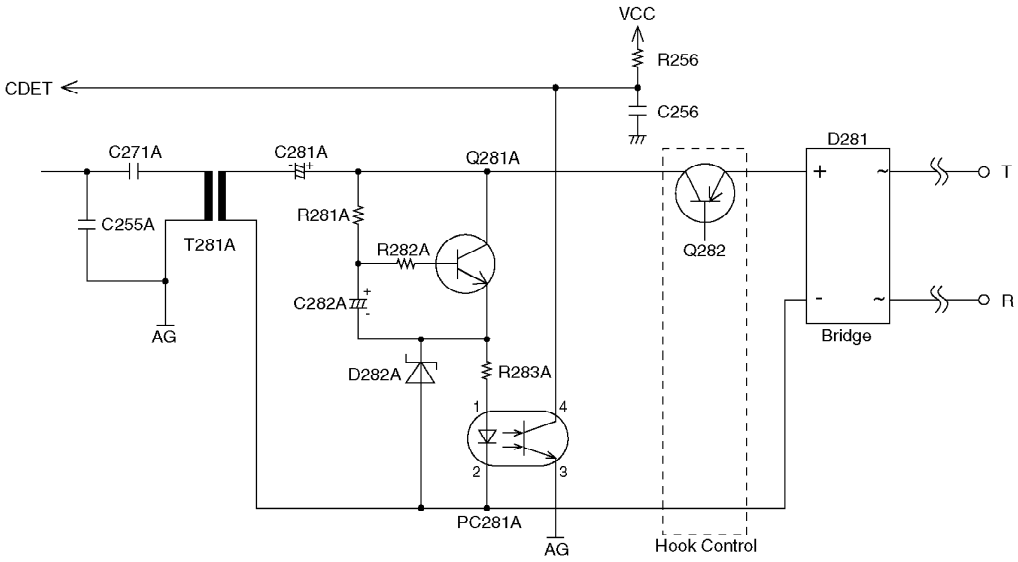
R253 → R252 → R249 → IC242 → R246

•Receive Voice Data

Transformer → R247A → IC244 - 2 → IC244 - 1 → Amplifier

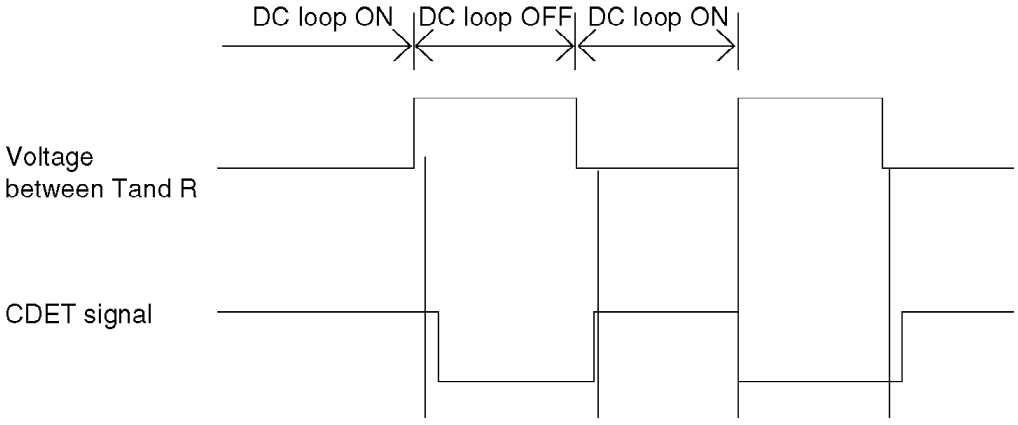
16.2.5. CPC DETECTOR

CPC Detector



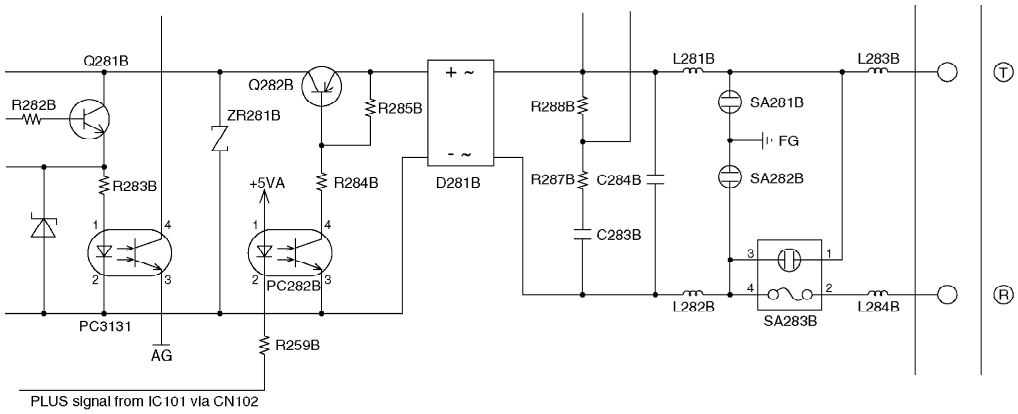
This logic detects the temporary disconnection of the DC loop current on the telephone line at off hook condition. The DC loop current flows through T ➞ D281 ➞ Q282 ➞ Q281 ➞ R283 ➞ PC281 - 1 ➞ PC281 - 2 ➞ D281 ➞ R. When DC loop is ON, photo coupler PC281 pin 4 - 3 is OFF and CDET signal drives to high. When DC loop is OFF, photo coupler PC281 pin 4 - 3 is on and CDET signal drives to low.

CPC Detector



16.2.6. HOOK CONTROL

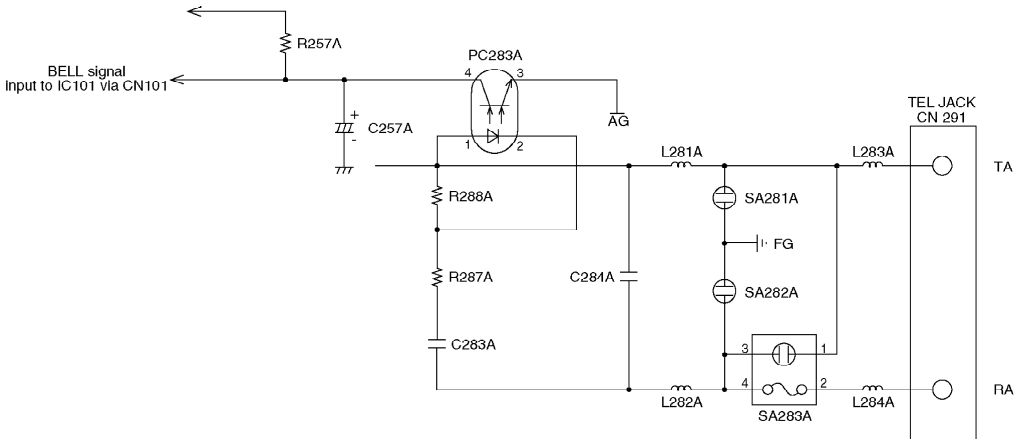
Hook Control



This logic controls the DC loop ON/OFF of the SLT interface. When ON hook condition, PLUS signal is driven to High Level by Co line control Port on IC101. In this condition, photo coupler PC282 pin 4 - 3 is ON and then Q282 is turn OFF. When OFF Hook condition, PLUS signal is driven to low level and then Q282 is turn on. As a result, the DC current flows through as the followings path.
DC loop path: T → L283 → L281 → D281 → Q282 → Q281 → R283 → PC281 → D281 → R286 → L282 → SA283 → L284 → R

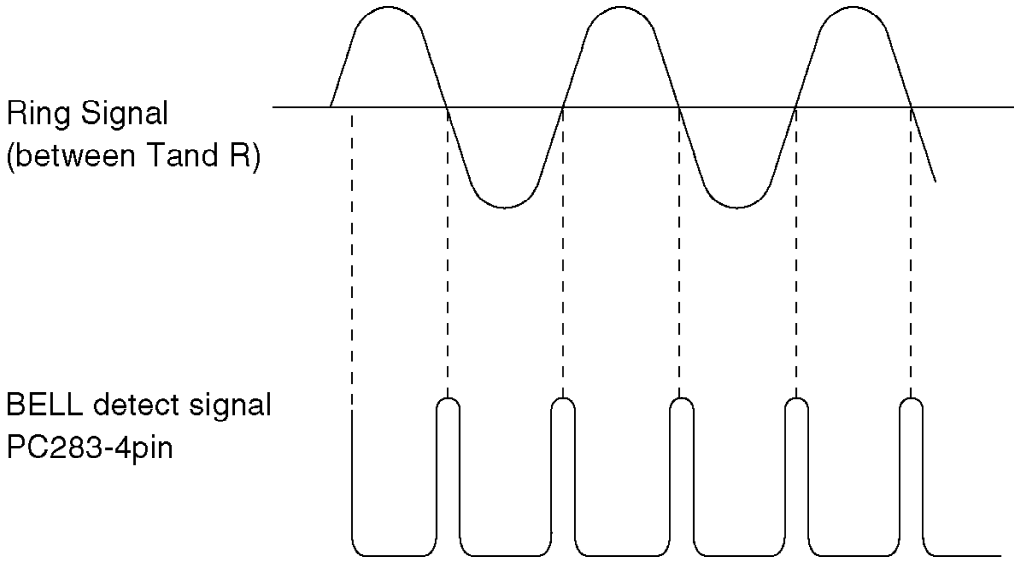
16.2.7. BELL DETECTOR

Bell Detector



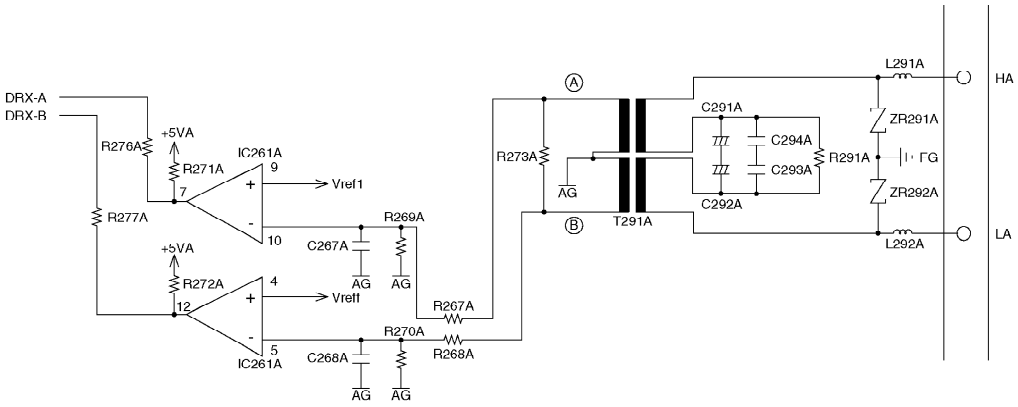
This logic detects the ringing status input form the SLT line at the ON Hook Condition. The ring signal flows through T → L283 → L281 → PC283 → R287 → C283 → L282 → SA283 → L283 → R.
If the ringing signal level over the threshold level of the PC281, photo coupler PC283 4 - 3 pin turn to ON. In this case, Bell signal is driven to low.

Bell Detector



16.2.8. DPT LINE RECEIVER

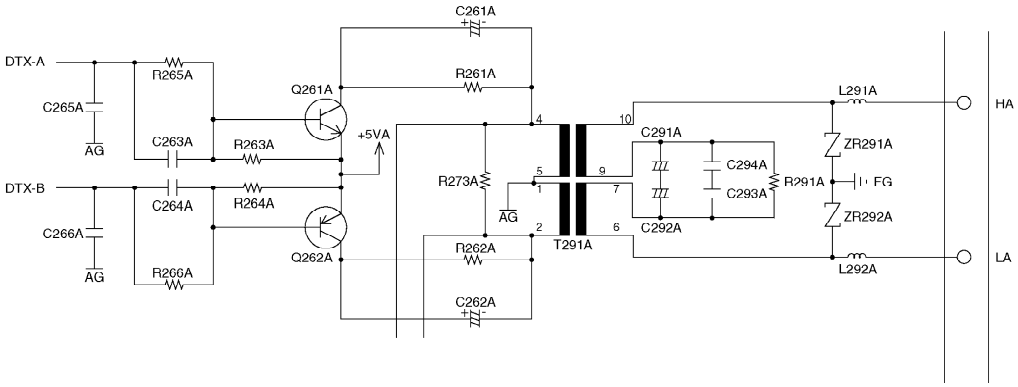
DPT Line Receiver



This logic allows to receive the D-PITS reception data from PBX.
The D-PITS reception data flows through HA ► L291A ► T291A (10 - 9) ► C291A ► C292A ► T291A (7 - 6) ► L292A.

16.2.9. DPT LINE TRANCEIVER

DPT Line Transceiver



This logic allows to transmit the D-PITS transmission data to PBX.
The D-PITS transmission signals flow through as the followings.

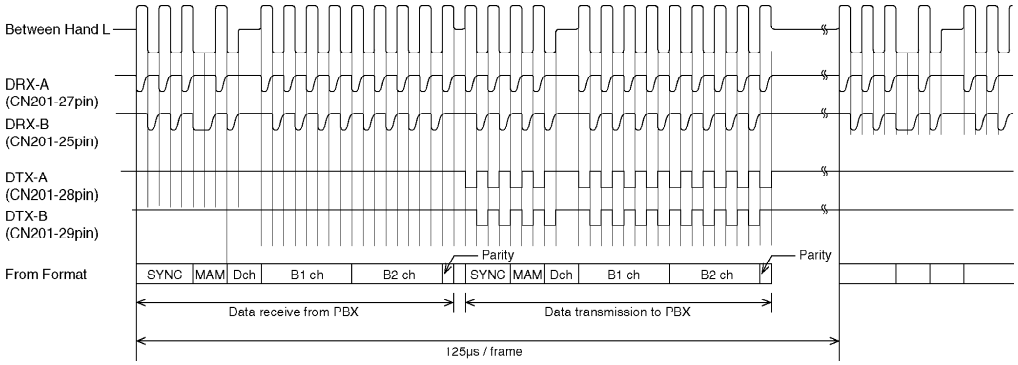
DTX - A = IC101 - 17 ► R113 ► CN102 - 28 ► R265A / C263A ► Base of Q261A.
DTX - B = IC101 - 18 ► R114 ► CN102 - 29 ► R266A / C264A ► Base of Q262A.

If IC101 drives DTX - A (DTX - B) to low level, Q261A (Q262A) is turn ON and the loop current flows through as the followings.

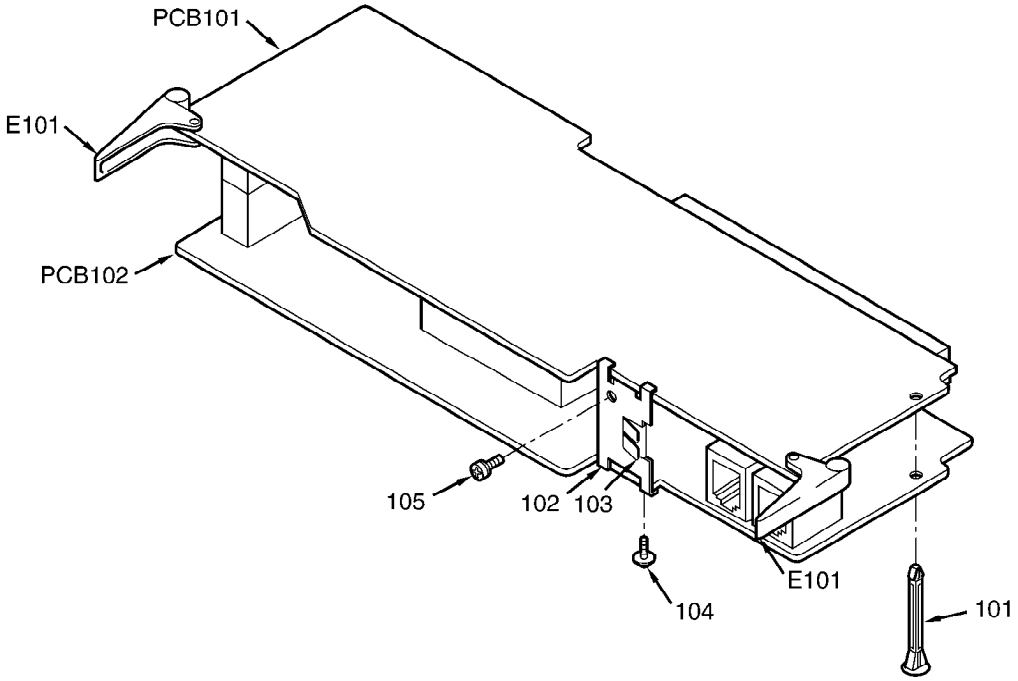
+5VA ► Q261A (C - E) ► R261A / C261A ► T291A (4 - 5) ► AG
+5VA ► Q262A (C - E) ► R261A / C262A ► T291A (2 - 1) ► AG

This loop current transition generates the D-PITS transmission data between T291A - 10 pin and T291A - 6pin. As a result,T291A drives the HA - LA line corresponding with DTX-A/DTX-B.

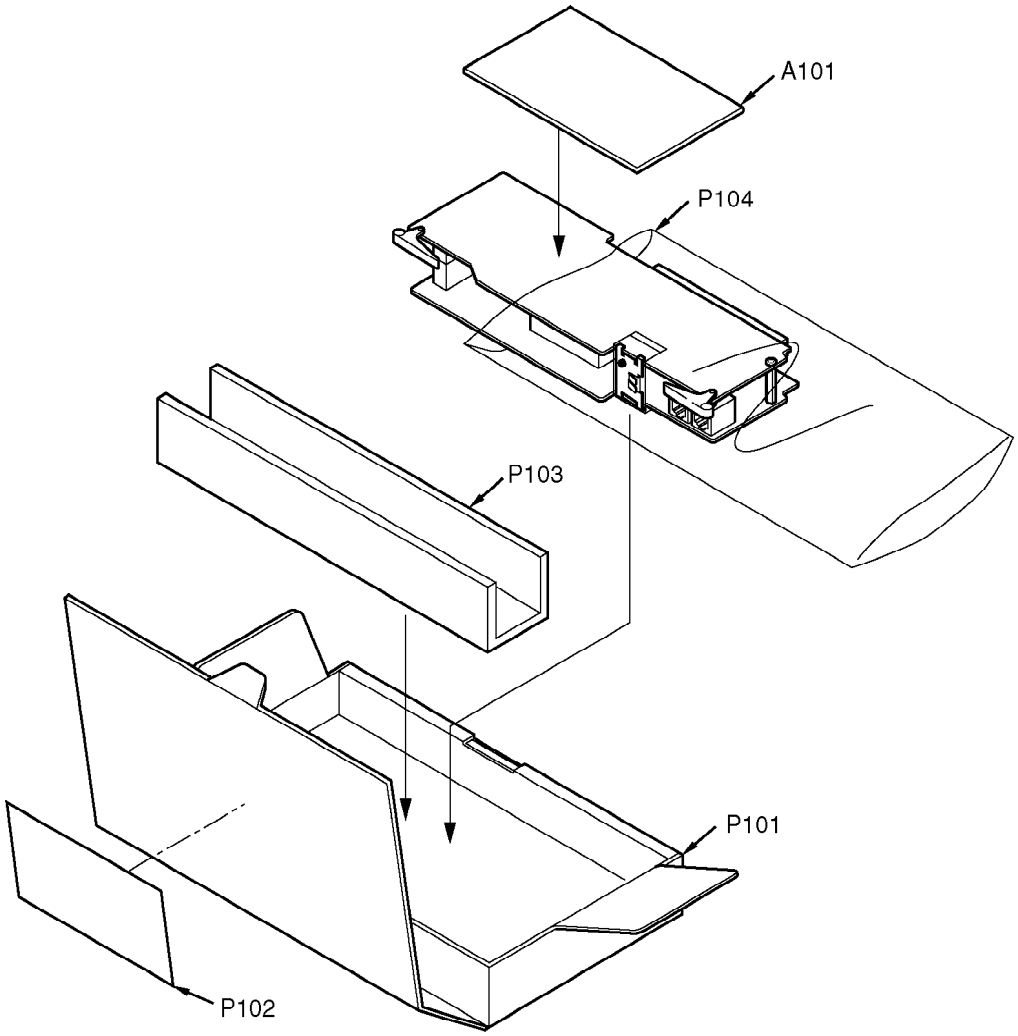
DPT Transmission



17. ELECTRICAL PARTS LOCATION (KX-TVS102)



18. ACCESSORIES AND PACKING MATERIAL (KX-TVS102)



19. REPLACEMENT PARTS LIST (KX-TVS102)(OPTION)

Note:

1. RTL (Retention Time Limited)

The marking (RTL) indicates that the Retention Time is limited for this item.

After the discontinuation of this assembly in production, the item will continue to be available for a specific period of time. The retention period of availability depends on the type of assembly and the laws governing parts and product retention. At the end of this period, the assembly will no longer be available.

2. Important safety notice

Components identified by the ⚠ mark indicates special characteristics important for safety. When replacing any of these

components, only use specified manufacture's parts.

3. The S mark means the part is one of some identical parts. For that reason, it may be different from the installed part.

4. RESISTORS & CAPACITORS
   Unless otherwise specified;
   All resistors are in ohms (Ω), k=1000 Ω , M=1000k Ω
   All capacitors are in MICRO FARADS (μ F), p= μ (μ F)
   *Type & Wattage of Resistor

Type

ERC:Solid ERD:Carbon PQRD:Carbon	ERX:Metal Film ERG:Metal Oxide ER0:Metal Film	PQ4R:Carbon ERS:Fusible Resistor ERF:Cement Resistor

Wattage

10,16:1/8W	14,25:1/4W	12:1/2W	1:1W	2:2W	3:3W

*Type & Voltage of Capacitor
Type

ECFD:Semi-Conductor ECQS:Styrol PQCUV:Chip ECQMS:Mica	ECCD,ECKD,ECBT,PQCBC:Ceramic ECQE,ECQV,ECQG:Polyester ECEA,ECSZ:Electlytic ECQP:Polypropylene

Voltage

ECQ Type	ECQG ECQV Type	ECSZ Type	Others	
1H:50V 2A:100V 2E:250V 2H:500V	05:50V 1:100V 2:200V	0F:3.15V 1A:10V 1V:35V 0J:6.3V	0J :6.3V 1A :10V 1C :16V 1E,25:25V	1V :35V 50,1H:50V 1J :63V 2A :100V

19.1. ELECTRICAL PARTS

Ref. No.	Part No.	Part Name & Description	Remarks
101	PQHR10306Z	SPACER	
102	PQMH10151Z	ANGLE	
103	PQMH10152Z	SPRING	
104	XYN3+F6FU	SCREW	
105	XYN3+C6FN	SCREW	

19.2. ACCESSORY AND PACKING MATERIALS

Ref. No.	Part No.	Part Name & Description	Remarks
A101	PSQW1415Z	LEAFLET	
P101	PQPK10180Z	GIFT BOX	
P102	PSQA1005Z	MODEL NO. LABEL	
P103	PSPN1003Z	CUSHION	
P104	PQPP10004Z	PROTECTION COVER	

19.3. DSP CARD PARTS

Ref. No.	Part No.	Part Name & Description	Remarks
PCB101	PQWP1VP100BX	DSP CARD ASS'Y (RTL)	
		(ICs)	
IC101	PQVIPD656214	IC	
IC102	PQVISN7L244S	IC	
IC103	PQVISN7L244S	IC	
IC104	PQVISN7L245S	IC	
IC105	PQVISN7L241M	IC	S
IC106	PQVISN7L126A	IC	
IC109A	PSVI8C060BPJ	IC	
IC109B	PSVI8C060BPJ	IC	
		(TRANSISTOR)	
Q100	PQVTDTC143E	TRANSISTOR(SI)	
		(CONNECTORS)	
CN101	PQJP50S33Z	CONNECTOR, 50P	
CN102	PQJP30A86Z	CONNECTOR, 30P	
		(CAPACITORS)	
C100	ECUV1H102KBV	0.001	
C101	ECUV1H102KBV	0.001	
C102	ECUV1H120JCV	12p	
C103	ECUV1H120JCV	12p	
C104	ECUV1H104ZFV	0.1	
C105	ECUV1H104ZFV	0.1	
C106	ECUV1H101JCV	100p	
C107	ECUV1H101JCV	100p	
C108	ECUV1H102KBV	0.001	
C109	ECUV1H102KBV	0.001	
C110	ECUV1H102KBV	0.001	
C111	ECUV1H102KBV	0.001	
C112	ECUV1H102KBV	0.001	
C113	ECUV1H102KBV	0.001	
C114A	ECUV1H102KBV	0.001	
C114B	ECUV1H102KBV	0.001	
C115A	ECUV1H104ZFV	0.1	
C115B	ECUV1H104ZFV	0.1	
C116A	PQCUV1H223KB	0.022	
C116B	PQCUV1H223KB	0.022	
C117A	ECUV1C391JCV	390p	
C117B	ECUV1C391JCV	390p	
C118A	ECUV1H104ZFV	0.1	
C118B	ECUV1H104ZFV	0.1	
C119A	PQCUV1H105JC	1	S
C119B	PQCUV1H105JC	1	S
C120A	ECUV1H104ZFV	0.1	
C120B	ECUV1H104ZFV	0.1	
C121A	ECUV1H104ZFV	0.1	
C121B	ECUV1H104ZFV	0.1	
C122A	ECUV1H104ZFV	0.1	
C122B	ECUV1H104ZFV	0.1	
C123A	ECUV1H104ZFV	0.1	
C123B	ECUV1H104ZFV	0.1	

Ref. No.	Part No.	Part Name & Description	Remarks
C180	ECEA1AKS221	220	
C181	PQCUV1H105JC	1	S
C182	PQCUV1H105JC	1	S
C183	PQCUV1H105JC	1	S
C184	PQCUV1H105JC	1	S
C185	ECUV1H104ZFV	0.1	
C186	ECUV1H104ZFV	0.1	
C187	ECUV1H104ZFV	0.1	
C188	ECUV1H104ZFV	0.1	
C189	ECUV1H104ZFV	0.1	
		(RESISTORS)	
R100	ERJ3GEYJ330	33	
R101	ERJ3GEYJ330	33	
R102	ERJ3GEYJ330	33	
R103	ERJ3GEYJ330	33	
R105	ERJ3GEYJ473	47k	
R106	ERJ3GEYJ473	47k	
R107	ERJ3GEY0R00	0k	
R108	ERJ3GEYJ221	220	
R110	ERJ3GEYJ330	33	
R111	ERJ3GEYJ330	33	
R112	ERJ3GEYJ330	33	
R113	ERJ3GEYJ330	33	
R114	ERJ3GEYJ330	33	
R115A	ERJ3GEYJ473	47k	
R115B	ERJ3GEYJ473	47k	
R116A	ERJ3GEYJ272	2.7k	
R116B	ERJ3GEYJ272	2.7k	
R117A	ERJ3GEYJ473	47k	
R117B	ERJ3GEYJ473	47k	
R118A	ERJ3GEYJ473	47k	
R118B	ERJ3GEYJ473	47k	
R119A	ERJ3GEYJ473	47k	
R119B	ERJ3GEYJ473	47k	
R120A	ERJ3GEYJ473	47k	
R120B	ERJ3GEYJ473	47k	
R121A	ERJ3GEYJ473	47k	
R121B	ERJ3GEYJ473	47k	
R122A	ERJ3GEYJ473	47k	
R122B	ERJ3GEYJ473	47k	
R123A	ERJ3GEYJ473	47k	
R123B	ERJ3GEYJ473	47k	
R124A	ERJ3GEYJ473	47k	
R124B	ERJ3GEYJ473	47k	
R125A	ERJ3GEYJ473	47k	
R125B	ERJ3GEYJ473	47k	
R126A	ERJ3GEYJ473	47k	
R126B	ERJ3GEYJ473	47k	
R127A	ERJ3GEYJ473	47k	
R127B	ERJ3GEYJ473	47k	
R128A	ERJ3GEYJ473	47k	
R128B	ERJ3GEYJ473	47k	
R129A	ERJ3GEYJ473	47k	

Ref. No.	Part No.	Part Name & Description	Remarks
R129B	ERJ3GEYJ473	47k	
R130A	ERJ3GEYJ473	47k	
R130B	ERJ3GEYJ473	47k	
R131A	ERJ3GEYJ473	47k	
R131B	ERJ3GEYJ473	47k	
R132A	ERJ3GEYJ473	47k	
R132B	ERJ3GEYJ473	47k	
R141	ERJ3GEYJ473	47k	
R142A	ERJ3GEYJ473	47k	
R142B	ERJ3GEYJ473	47k	
		(CRYSTAL OSCILLATOR)	
X100	PQVCJ16384N8	CRYSTAL OSCILLATOR	
		(OTHERS)	
E101	PQHR10207Z	LEVER	

19.4. CO CARD PARTS

Ref. No.	Part No.	Part Name & Description	Remarks
PCB102	PQWP2VP100BX	CO CARD ASS'Y (RTL)	
		(ICs)	
IC241A	PQVIMP58C20D	IC	
IC241B	PQVIMP58C20D	IC	
IC242A	PQVINJM2058V	IC	
IC242B	PQVINJM2058V	IC	
IC243A	PQVITC4S66F	IC	
IC243B	PQVITC4S66F	IC	
IC244A	PQVITC4S66F	IC	
IC244B	PQVITC4S66F	IC	
IC261A	PQVINJM319V	IC	
		(TRANSISTORS)	
Q212	PQVTDTC143E	TRANSISTOR(SI)	
Q213	PQVTDTA143EU	TRANSISTOR(SI)	
Q261A	2SA1576Q	TRANSISTOR(SI)	⚠
Q261B	2SA1576Q	TRANSISTOR(SI)	⚠
Q281A	2SD2040	TRANSISTOR(SI)	⚠
Q281B	2SD2040	TRANSISTOR(SI)	⚠
Q282A	2SA1627	TRANSISTOR(SI)	⚠
Q282B	2SA1627	TRANSISTOR(SI)	⚠
		(DIODES)	
D281A	PQVDS1ZB60F1	DIODE(SI)	⚠
D281B	PQVDS1ZB60F1	DIODE(SI)	⚠
D282A	PQVDHZS2B1	DIODE(SI)	⚠
D282B	PQVDHZS2B1	DIODE(SI)	⚠
		(CONNECTOR & JACK)	
CN201	PQJS30A53Z	CONNECTOR, 30P	

Ref. No.	Part No.	Part Name & Description	Remarks
CN291	PQJJ2T003Z	JACK, TEL	
		(CAPACITORS)	
C201	ECEA1AU221	220	
C202	ECEA1AU221	220	
C230A	PQCUV1H223KB	0.022	
C231A	PQCUV1H223KB	0.022	
C231B	PQCUV1H223KB	0.022	
C233A	PQCUV1H223KB	0.022	
C233B	PQCUV1H223KB	0.022	
C234A	PQCUV1H223KB	0.022	
C235A	PQCUV1H223KB	0.022	
C235B	PQCUV1H223KB	0.022	
C237A	PQCUV1H223KB	0.022	
C237B	ECUV1H223KBV	0.022	
C241A	PQCUV1E104MD	0.1	
C241B	PQCUV1E104MD	0.1	
C242A	PQCUV1E104MD	0.1	
C242B	PQCUV1E104MD	0.1	
C244A	PQCUV1H101JC	100p	
C244B	PQCUV1H101JC	100p	
C245A	PQCUV1E104MD	0.1	
C245B	PQCUV1E104MD	0.1	
C246A	PQCUV1E104MD	0.1	
C246B	PQCUV1E104MD	0.1	
C247A	PQCUV1H101JC	100p	
C247B	PQCUV1H101JC	100p	
C248A	PQCUV1H101JC	100p	
C248B	PQCUV1H101JC	100p	
C249A	PQCUV1H101JC	100p	
C249B	PQCUV1H101JC	100p	
C250A	PQCUV1H103KB	0.01	
C250B	PQCUV1H103KB	0.01	
C255A	PQCUV1H102J	0.001	
C255B	PQCUV1H102J	0.001	
C256A	PQCUV1H103KB	0.01	
C256B	PQCUV1H103KB	0.01	
C257A	ECEA1HUR47	0.47	
C257B	ECEA1HUR47	0.47	
C261A	ECEA1HKA010	1	
C262A	ECEA1HKA010	1	
C263A	PQCUV1H680JC	68p	
C264A	PQCUV1H680JC	68p	
C265A	PQCUV1H101JC	100p	
C266A	PQCUV1H101JC	100p	
C267A	PQCUV1H470JC	47p	
C268A	PQCUV1H470JC	47p	
C269A	PQCUV1H223KB	0.022	S
C270A	PQCUV1H101JC	100p	
C270B	PQCUV1H101JC	100p	
C271A	ECUV1C105KB	1	
C271B	ECUV1C105KB	1	
C272A	PQCUV1H223KB	0.022	S
C272B	PQCUV1H223KB	0.022	S

Ref. No.	Part No.	Part Name & Description	Remarks
C281A	ECEA1HU100	10	
C281B	ECEA1HU100	10	
C282A	ECEA1HU100	10	
C282B	ECEA1HU100	10	
C283A	ECQE2E474KZ	0.47	⚠
C283B	ECQE2E474KZ	0.47	⚠
C284A	ECKDKC222KB	0.0022	S ⚠
C284B	ECKDKC222KB	0.0022	S ⚠
C291A	ECEA1HN4R7S	4.7	
C292A	ECEA1HN4R7S	4.7	
		(COILS)	
L201	PQLQR1T2R2M	COIL	
L202	PQLQR1T2R2M	COIL	
L281A	PQLE106	COIL	⚠
L281B	PQLE106	COIL	⚠
L282A	PQLE106	COIL	⚠
L282B	PQLE106	COIL	⚠
L283A	PQLE106	COIL	⚠
L283B	PQLE106	COIL	⚠
L284A	PQLE106	COIL	⚠
L284B	PQLE106	COIL	⚠
L291A	PQLQR1LT	COIL	⚠
L292A	PQLQR1LT	COIL	⚠
		(PHOTO ELECTRIC TRANSDUCERS)	
PC281A	PQVIPC817K	PHOTO COUPLER	⚠ S
PC281B	PQVIPC817K	PHOTO COUPLER	⚠ S
PC282A	PQVITLP627	PHOTO COUPLER	⚠
PC282B	PQVITLP627	PHOTO COUPLER	⚠
PC283A	0N3181R	PHOTO COUPLER	⚠
PC283B	0N3181R	PHOTO COUPLER	⚠
		(RESISTORS)	
R211	PQ4R10XJ000	0	
R212	PQ4R10XJ000	0	
R213	PQ4R10XJ000	0	
R214	PQ4R10XJ000	0	
R215	PQ4R10XJ472	4.7k	
R216	PQ4R10XJ472	4.7k	
R223	ERJ3GEYJ101	100	
R224	ERJ3GEYJ101	100	
R225	ERJ3GEYJ101	100	
R226	ERJ3GEYJ101	100	
R227	PQ4R10XJ101	100	
R228	PQ4R10XJ101	100	
R229	PQ4R10XJ101	100	
R230	PQ4R10XJ101	100	
R231A	PQ4R10XF1203	120k	
R231B	PQ4R10XF1203	120k	
R232A	PQ4R10XF4702	47k	

Ref. No.	Part No.	Part Name & Description	Remarks
R232B	PQ4R10XF4702	47k	
R233A	PQ4R10XF4702	47k	
R233B	PQ4R10XF4702	47k	
R234A	PQ4R10XF1203	120k	
R234B	PQ4R10XF1203	120k	
R235A	PQ4R10XF1003	100k	
R235B	PQ4R10XF1003	100k	
R241A	PQ4R10XF1203	120k	
R241B	PQ4R10XF1203	120k	
R242A	PQ4R10XF4702	47k	
R242B	PQ4R10XF4702	47k	
R243A	PQ4R10XF1003	100k	
R243B	PQ4R10XF1003	100k	
R244A	PQ4R10XF2323	232k	
R244B	PQ4R10XF2323	232k	
R245A	PQ4R10XJ394	390k	
R245B	PQ4R10XJ394	390k	
R246A	PQ4R10XF4702	47k	
R246B	PQ4R10XF4702	47k	
R247A	PQ4R10XF4702	47k	
R247B	PQ4R10XF4702	47k	
R248A	PQ4R10XF1003	100k	
R248B	PQ4R10XF1003	100k	
R249A	PQ4R10XF1003	100k	
R249B	PQ4R10XF1003	100k	
R250A	PQ4R10XF6800	680	
R250B	PQ4R10XF6800	680	
R251A	PQ4R10XF3900	390	
R251B	PQ4R10XF3900	390	
R252A	PQ4R10XJ000	0	
R252B	PQ4R10XJ000	0	
R253A	PQ4R10XF1211	1.21k	
R253B	PQ4R10XF1211	1.21k	
R254A	PQ4R10XJ000	0	
R254B	PQ4R10XJ000	0	
R255A	PQ4R10XF1211	1.21k	
R255B	PQ4R10XF1211	1.21k	
R256A	PQ4R10XJ104	100k	
R256B	PQ4R10XJ104	100k	
R257A	PQ4R10XJ104	100k	
R257B	ERJ3GEYJ104	100k	
R258A	PQ4R10XJ104	100k	
R258B	ERJ3GEYJ104	100k	
R259A	PQ4R10XJ102	1k	
R259B	PQ4R10XJ102	1k	
R260A	PQ4R10XF1003	100k	
R260B	PQ4R10XF1003	100k	
R261A	PQ4R10XJ330	33	
R262A	PQ4R10XJ330	33	
R263A	PQ4R10XJ472	4.7k	
R264A	PQ4R10XJ472	4.7k	
R265A	PQ4R10XJ472	4.7k	
R266A	PQ4R10XJ472	4.7k	
R267A	PQ4R10XJ472	4.7k	

Ref. No.	Part No.	Part Name & Description	Remarks
R268A	PQ4R10XJ472	4.7k	
R269A	PQ4R10XJ472	4.7k	
R270A	PQ4R10XJ472	4.7k	
R271A	PQ4R10XJ472	4.7k	
R272A	PQ4R10XJ472	4.7k	
R273A	PQ4R10XJ821	820	
R274A	PQ4R10XF8201	8.2k	
R275A	PQ4R10XF1201	1.2k	
R276A	PQ4R10XJ330	33	
R277A	PQ4R10XJ330	33	
R281A	ERDS2TJ822	8.2k	
R281B	ERDS2TJ822	8.2k	
R282A	ERDS2TJ222	2.2k	
R282B	ERDS2TJ222	2.2k	
R283A	ERDS2TJ390	39	
R283B	ERDS2TJ390	39	
R284A	ERDS2TJ472	4.7k	
R284B	ERDS2TJ472	4.7k	
R285A	ERDS2TJ104	100k	
R285B	ERDS2TJ104	100k	
R286A	PQRQ25VJ5R6	5.6	
R286B	PQRQ25VJ5R6	5.6	
R287A	ERQN1VJ223	22k	
R287B	ERQN1VJ223	22k	
R288A	ERDS2TJ122	1.2k	
R288B	ERDS2TJ122	1.2k	
R291A	ERQS1TJ681	680k	
		(VARISTORS)	
SA280	PQVDDSSV301Y	VARISTOR (SURGE ABSORBER)	⚠
SA281A	PQVDRA311PT3	VARISTOR (SURGE ABSORBER)	⚠
SA281B	PQVDRA311PT3	VARISTOR (SURGE ABSORBER)	⚠
SA282A	PQVDRA311PT3	VARISTOR (SURGE ABSORBER)	⚠
SA282B	PQVDRA311PT3	VARISTOR (SURGE ABSORBER)	⚠
SA283A	PQVDDSSV301Y	VARISTOR (SURGE ABSORBER)	⚠
SA283B	PQVDDSSV301Y	VARISTOR (SURGE ABSORBER)	⚠
ZR281A	ERZC07DK820	VARISTOR	⚠
ZR281B	ERZC07DK820	VARISTOR	⚠
ZR291A	ERZC07DK820	VARISTOR	⚠
ZR292A	ERZC07DK820	VARISTOR	⚠
		(TRANSFORMERS)	
T281A	ETA14Y184AY	TRANSFORMER	⚠
T281B	ETA14Y184AY	TRANSFORMER	⚠
T291A	ETE13K79AY	TRANSFORMER	⚠

20. NOTES FOR SCHEMATIC DIAGRAM

1. DC voltage measurements are taken with an electronic voltmeter and oscilloscope from a ground line.

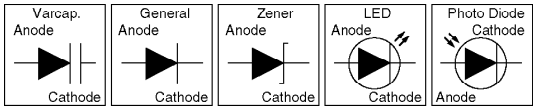
- Power Switch ON condition
- Voltage Value : V

2. This schematic diagram may be modified at any time with the development of new technology.

3.

Important safety notice The shaded area on this schematic diagram incorporates special features important for protection from fire and electrical shock hazards. When servicing it is essential that only manufacturer's specified parts be used for the critical components in the shaded areas of the schematic.

4.



21. WAVEFORM

21.1. MAIN BOARD

21.2. POWER SUPPLY BOARD

22. SCHEMATIC DIAGRAM

22.1. MAIN BOARD

22.2. DPT INTERFACE CARD(KX-TVS204)

22.2.1. DPT INTERFACE CARD(KX-TVS204)(NO.1,NO.2)

22.2.2. DPT INTERFACE CARD(KX-TVS204)(NO.3,NO.4)

22.3. POWER SUPPLY BOARD

22.4. CO CARD (KX-TVS102)(OPTION)

22.5. DPS CARD (KX-TVS102)(OPTION)

23. PRINTED CIRCUIT BOARD

23.1. MAIN BOARD

23.1.1. COMPONENT VIEW

23.1.2. BOTTOM VIEW

23.2. DPT INTERFACE CARD(KX-TVS204)

23.2.1. COMPONENT VIEW

23.2.2. BOTTOM VIEW

23.3. POWER SUPPLY BOARD

23.4. KX-TVS102(DSP CARD)(OPTION)

23.4.1. COMPONENT VIEW

23.4.2. BOTTOM VIEW

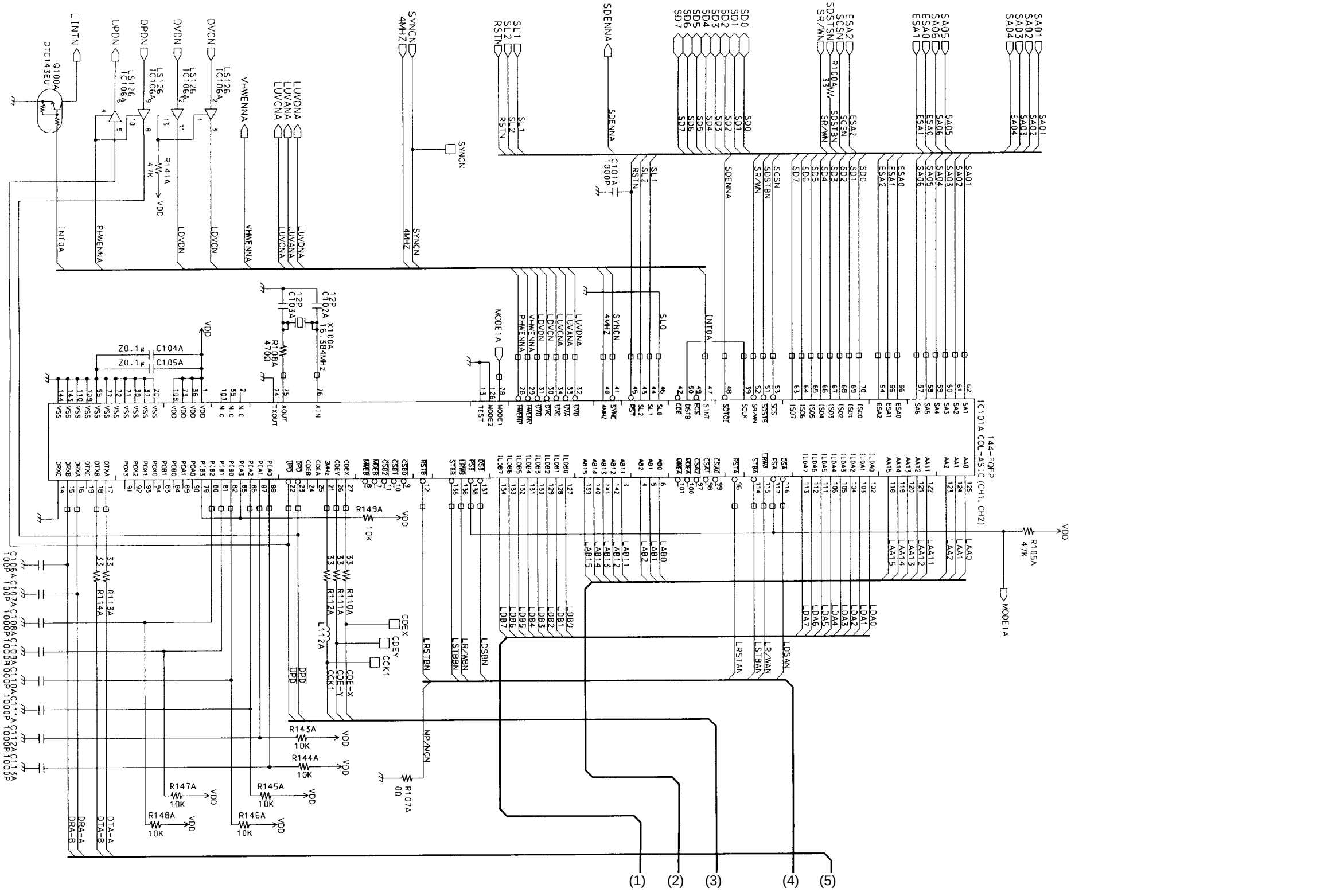
23.5. KX-TVS102(CO CARD)(OPTION)

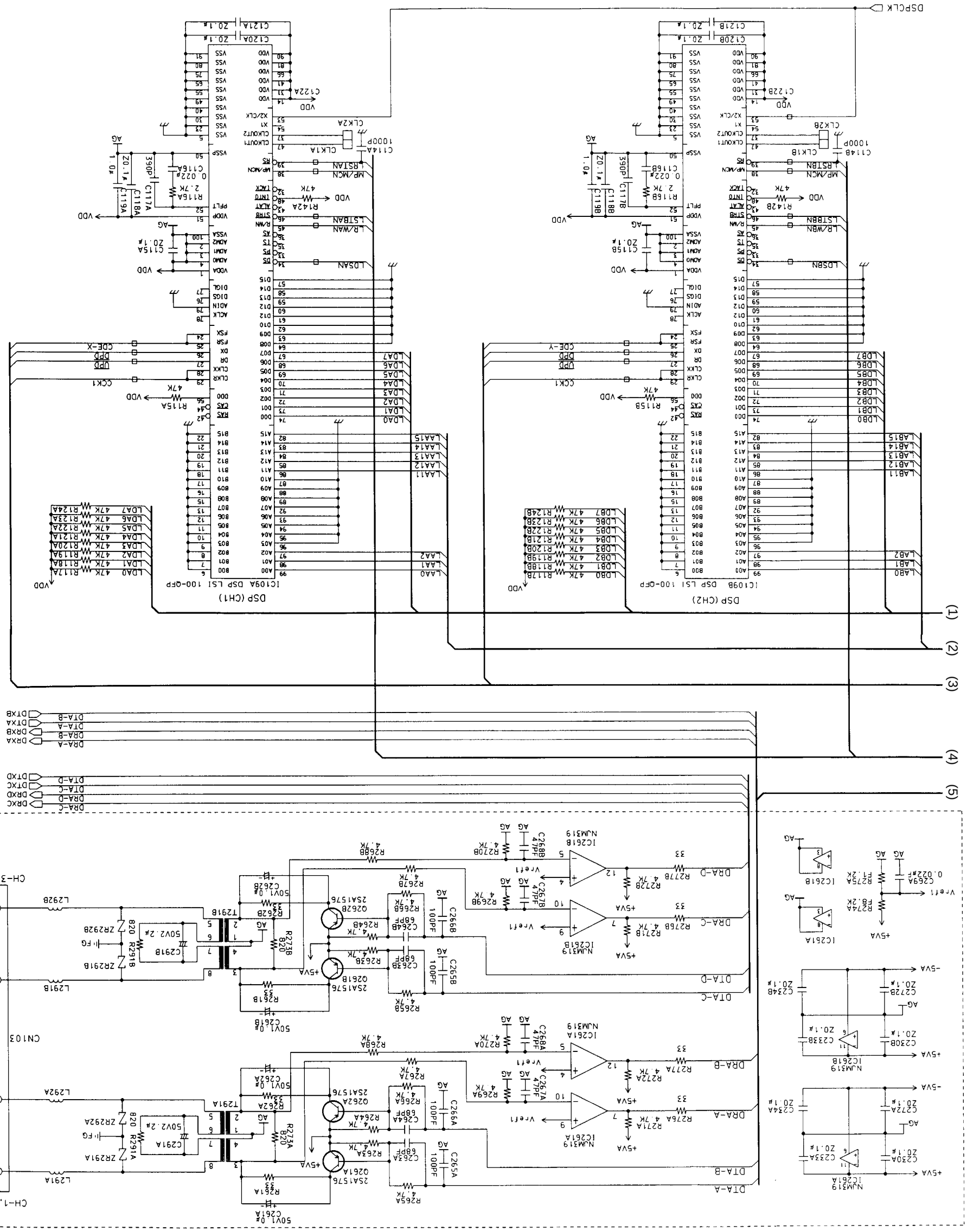
23.5.1. COMPONENT VIEW

23.5.2. BOTTOM VIEW

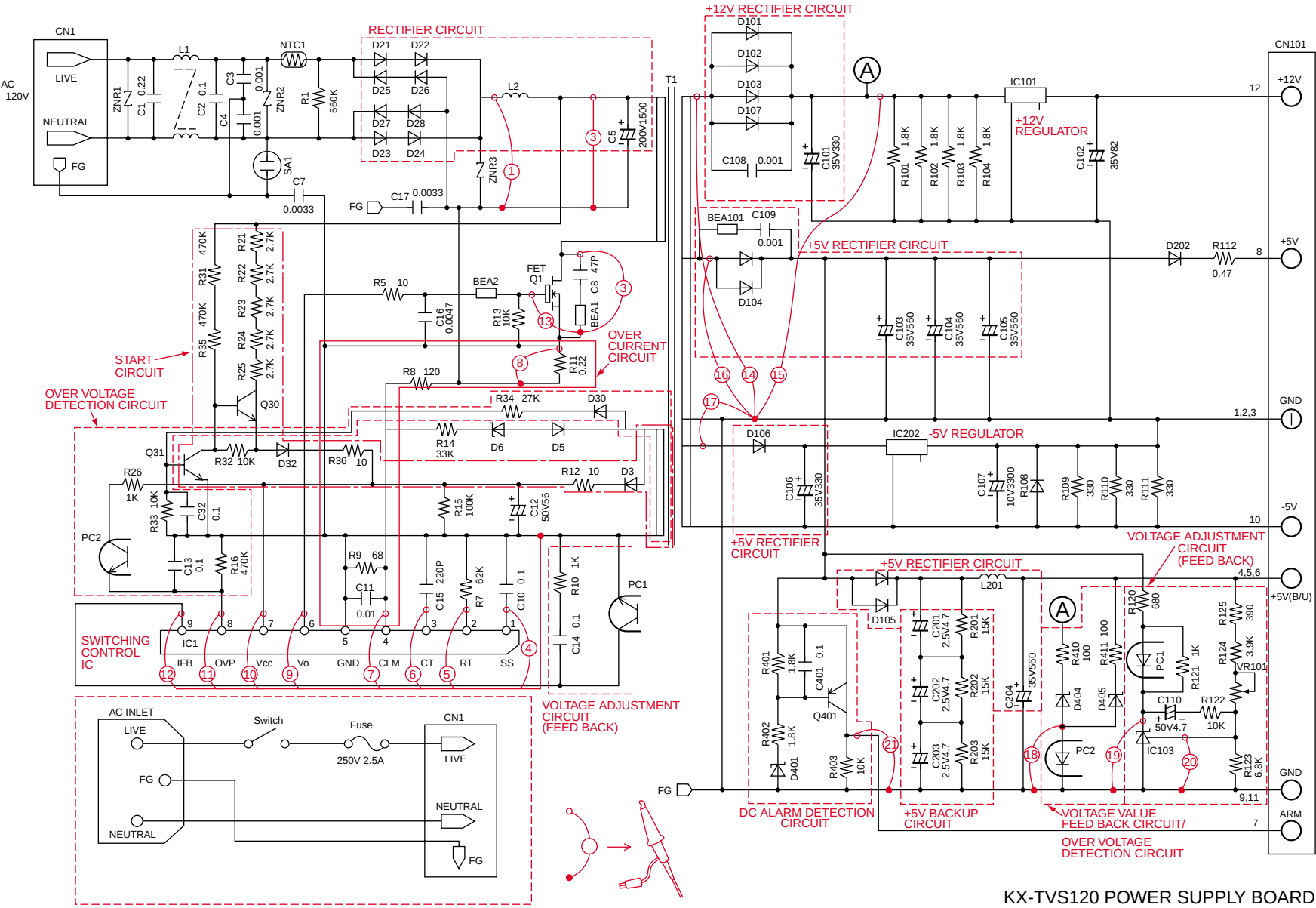
24. SCHEMATIC DIAGRAM FOR PRINTING WITH A4 SIZE

A KXTVS120

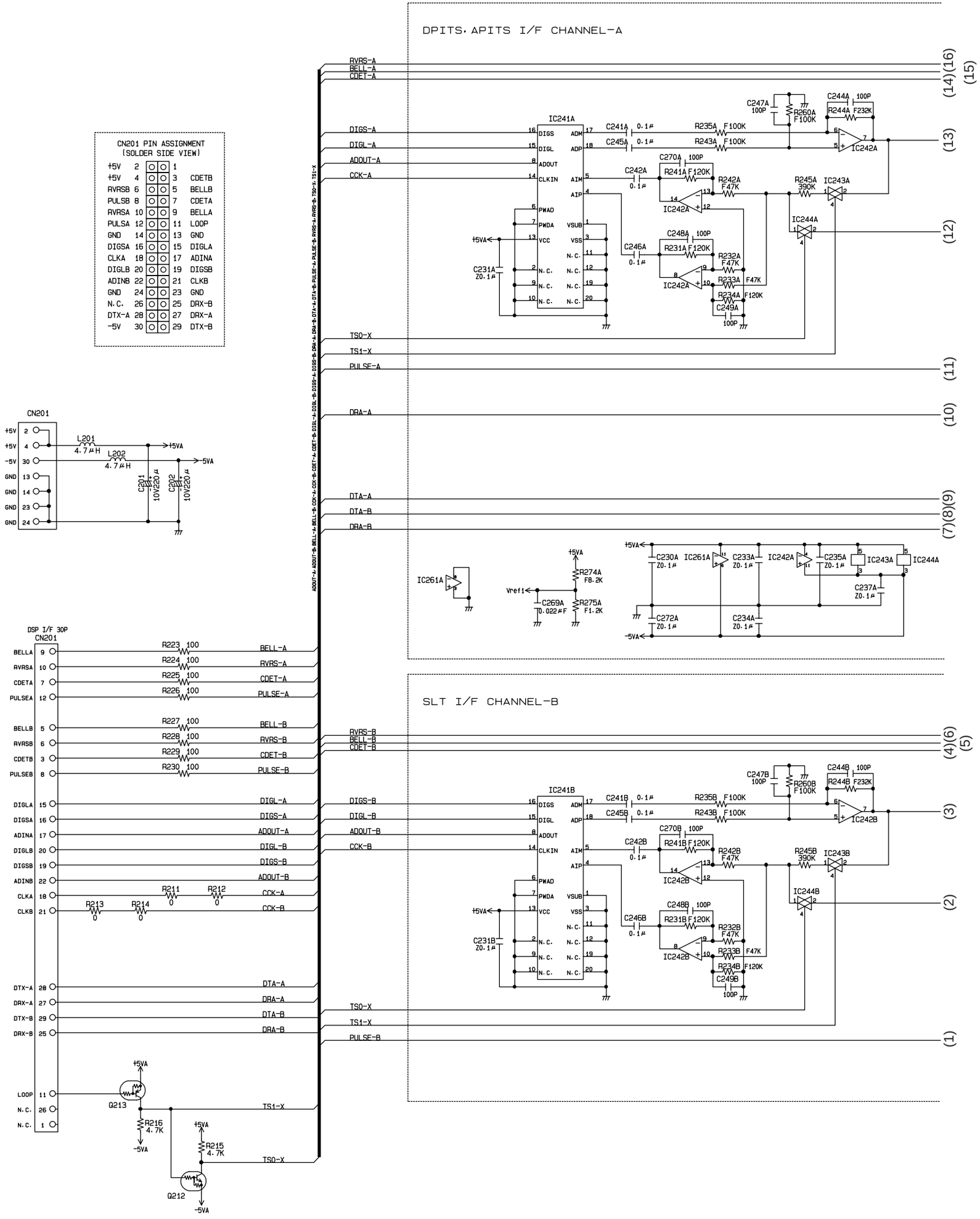

IC101A 144-FQFP COL-ASIC (CH1, CH2)
SA01
SA02
SA03
SA04
SA05
SA06
ESA0
ESA1
ESA2
SCSN
SDSTBN
SR/WN
SD0
SD1
SD2
SD3
SD4
SD5
SD6
SD7
SDENNA
SYNCN
4MHZ
SL1
SL2
RSTN
INTOA
LINTN
Q100A DTC143EU
DVCN
DVDN
DPDN
UPDN
LS126 IC106A
R141A 47K
VDD
VHWENNA
LUVDNA
LUVANA
LUVCNA
LDVCN
LDVDN
PHWENNA
C101A 1000P
X100A 16.384MHz
12P C102A
12P C103A
R108A 470Ω
C104A
C105A
Z0.1μ
MODE1A
MODE2
TEST
XIN
XOUT
TXOUT
R105A 47K
MODE1A
R149A 10K
R143A 10K
R144A 10K
R147A 10K
R148A 10K
R145A 10K
R146A 10K
R107A 0Ω
MP/MCN
R110A
R111A
R112A
L112A
CDEX
CDEY
CCK1
CDE-X
CDE-Y
R113A 33
R114A 33
C106A 1000P
C107A 1000P
C108A 1000P
C109A 1000P
C110A 1000P
C111A 1000P
C112A 1000P
C113A 1000P
DRA-A
DRA-B
DTA-A
DTA-B
LRSTBN
LDSBN
LRSTAN
LDSAN
LR/WBN
LSTBBN
LR/WAN
LSTBAN
LAA0
LAA1
LAA2
LAA11
LAA12
LAA13
LAA14
LAA15
LAB0
LAB1
LAB2
LAB11
LAB12
LAB13
LAB14
LAB15
LDA0
LDA1
LDA2
LDA3
LDA4
LDA5
LDA6
LDA7
LDB0
LDB1
LDB2
LDB3
LDB4
LDB5
LDB6
LDB7
(1)
(2)
(3)
(4)
(5)

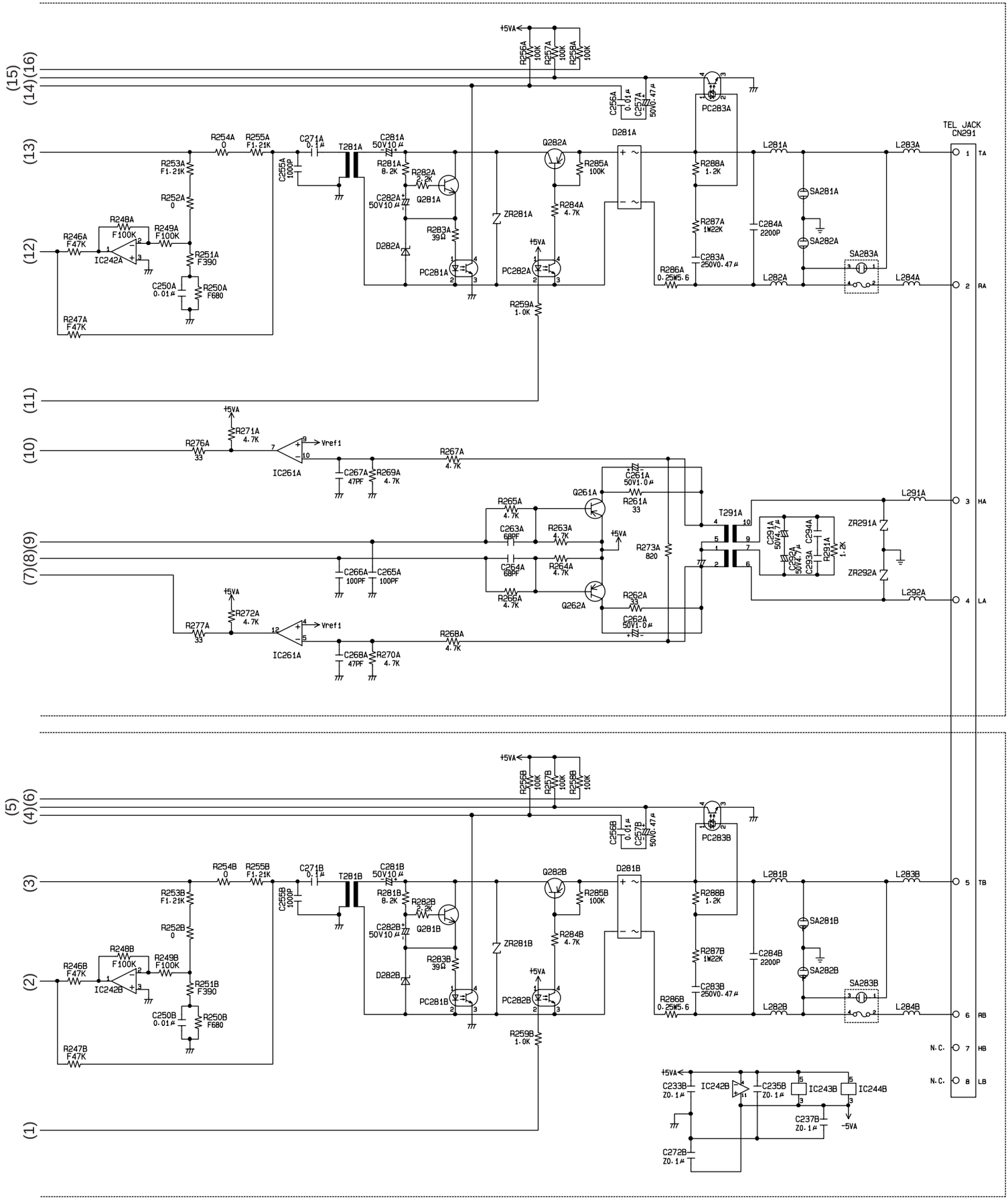


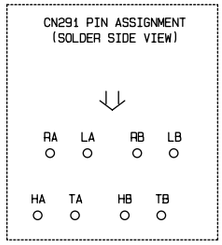
KX-TVS120 DPT INTERFACE CARD(KX-TVS204) No.4

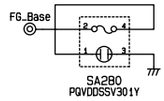


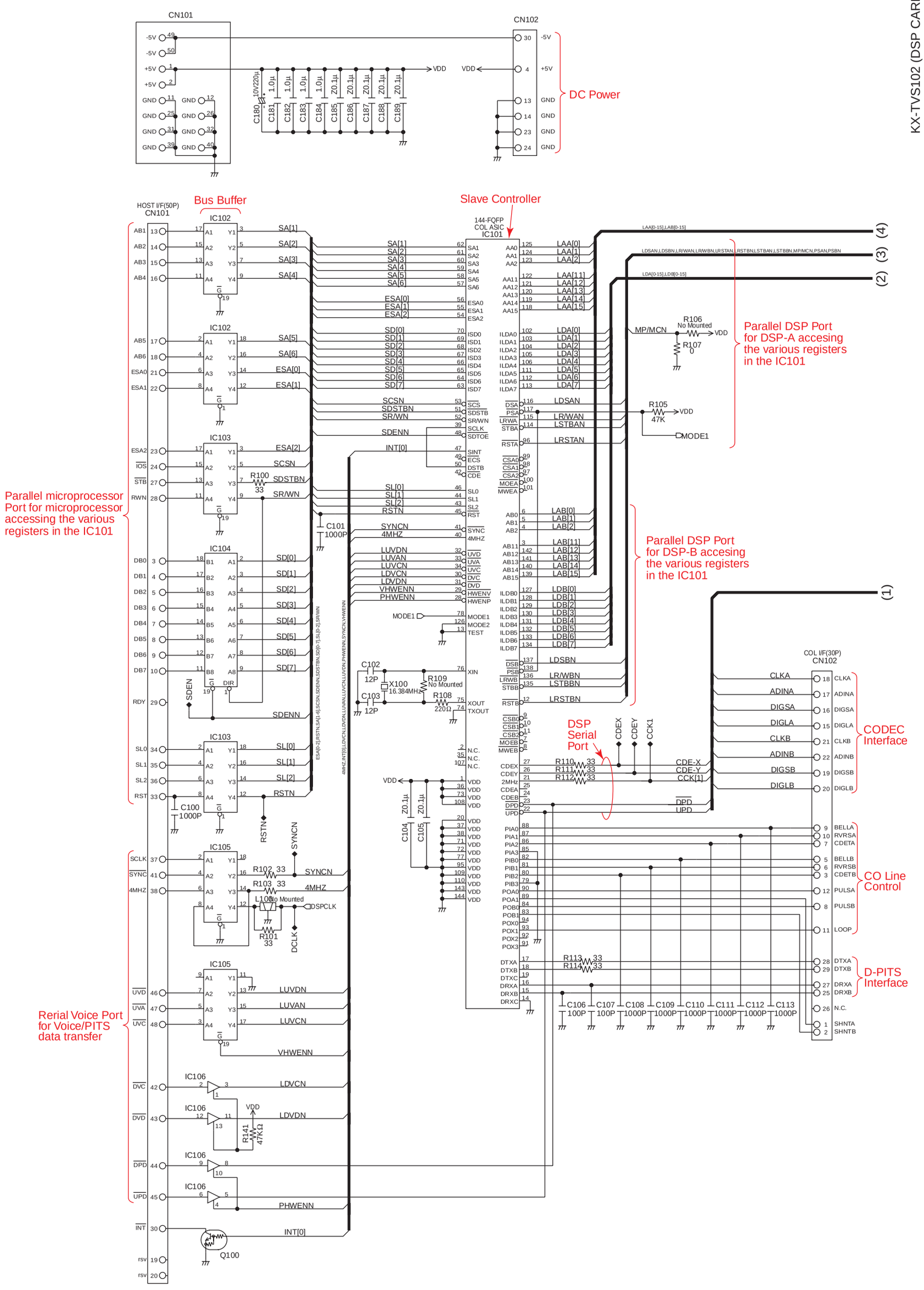
KX-TVS120 POWER SUPPLY BOARD

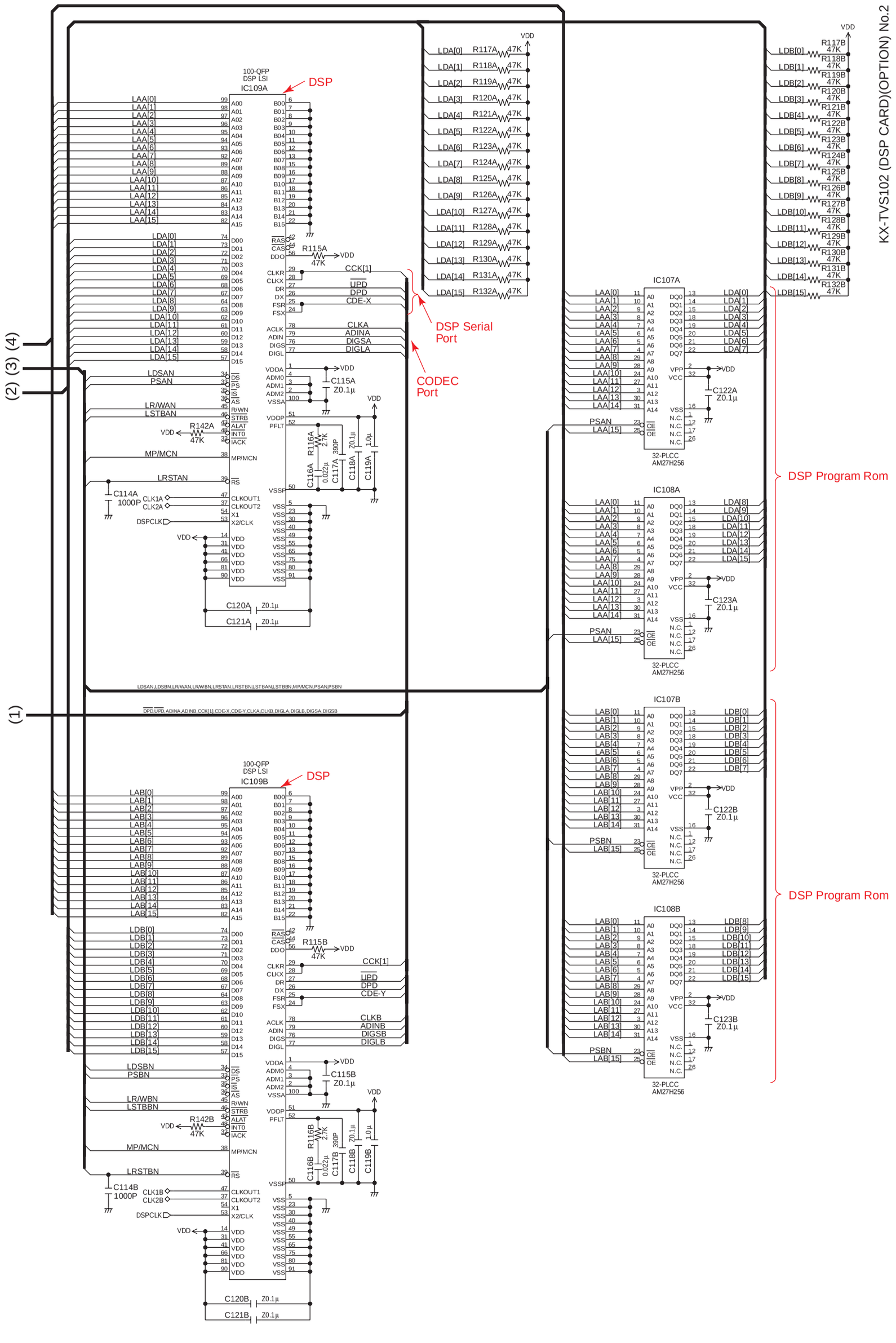

DPITS. APITS I/F CHANNEL-A
SLT I/F CHANNEL-B
CN201 PIN ASSIGNMENT (SOLDER SIDE VIEW)
+5V 2 1
+5V 4 3 CDETB
RVRSB 6 5 BELLB
PULSB 8 7 CDETA
RVRSA 10 9 BELLA
PULSA 12 11 LOOP
GND 14 13 GND
DIGSA 16 15 DIGLA
CLKA 18 17 ADINA
DIGLB 20 19 DIGSB
ADINB 22 21 CLKB
GND 24 23 GND
N.C. 26 25 DRX-B
DTX-A 28 27 DRX-A
-5V 30 29 DTX-B
RVRS-A
BELL-A
CDET-A
DIGS-A
DIGL-A
ADOUT-A
CCK-A
TS0-X
TS1-X
PULSE-A
DRA-A
DTA-A
DTA-B
DRA-B
RVRS-B
BELL-B
CDET-B
DIGS-B
DIGL-B
ADOUT-B
CCK-B
TS0-X
TS1-X
PULSE-B
IC241A
IC241B
IC242A
IC242B
IC243A
IC243B
IC244A
IC244B
IC261A
CN201
DSP I/F 30P
Q213
Q212
+5VA
-5VA
(14)(16)
(15)
(13)
(12)
(11)
(10)
(7)(8)(9)
(4)(6)
(5)
(3)
(2)
(1)

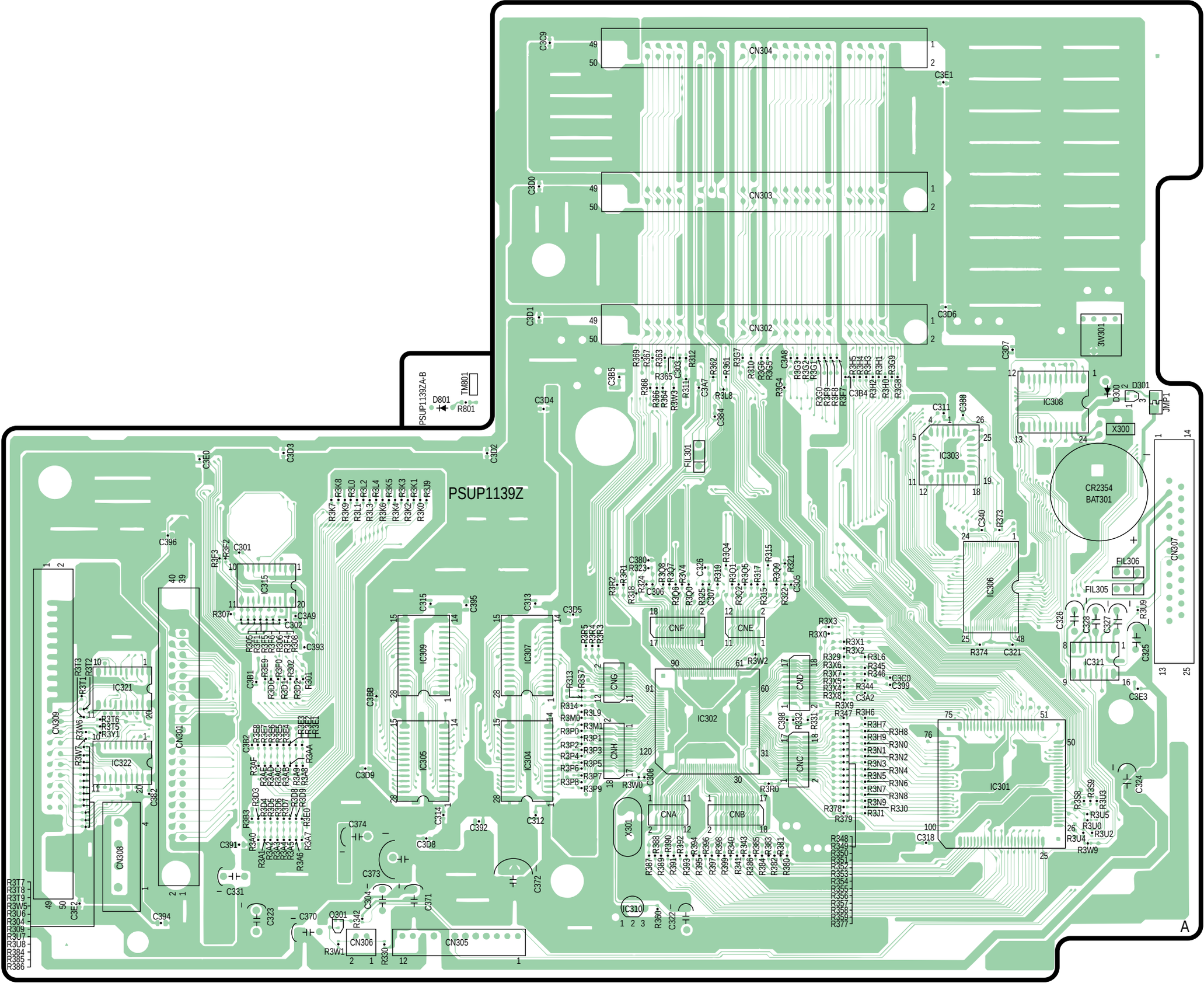

+5VA
R256A 100K
R257A 100K
R258A 100K
C256A 0.01μ
C257A 50V0.47μ
PC283A
D281A
TEL JACK CN291
(15)
(14)(16)
(13)
(12)
(11)
(10)
(7)(8)(9)
R254A 0
R255A F1.21K
C271A 0.1μ
T281A
C281A 50V10μ
R253A F1.21K
R252A 0
C255A 1000P
R248A F100K
R249A F100K
R246A F47K
IC242A
R251A F390
C250A 0.01μ
R250A F680
R247A F47K
R281A 8.2K
R282A 2.2K
C282A 50V10μ
Q281A
R283A 39Ω
D282A
PC281A
PC282A
Q282A
R285A 100K
R284A 4.7K
ZR281A
R259A 1.0K
R288A 1.2K
R287A 1W22K
C283A 250V0.47μ
R286A 0.25W5.6
L281A
L283A
L282A
L284A
C284A 2200P
SA281A
SA282A
SA283A
R271A 4.7K
R276A 33
IC261A
Vref1
C267A 47PF
R269A 4.7K
R267A 4.7K
R272A 4.7K
R277A 33
C268A 47PF
R270A 4.7K
R268A 4.7K
C261A 50V1.0μ
R261A 33
Q261A
R265A 4.7K
C263A 68PF
R263A 4.7K
C264A 68PF
R264A 4.7K
R266A 4.7K
Q262A
R262A 33
C262A 50V1.0μ
C266A 100PF
C265A 100PF
R273A 820
T291A
C291A 50V4.7μ
C292A 50V2.2μ
C294A
C293A
R291A 1.2K
ZR291A
ZR292A
L291A
L292A
1 TA
2 RA
3 HA
4 LA
(5)
(4)(6)
(3)
(2)
(1)
R256B 100K
R257B 100K
R258B 100K
C256B 0.01μ
C257B 50V0.47μ
PC283B
D281B
R254B 0
R255B F1.21K
C271B 0.1μ
T281B
C281B 50V10μ
R253B F1.21K
R252B 0
C255B 1000P
R248B F100K
R249B F100K
R246B F47K
IC242B
R251B F390
C250B 0.01μ
R250B F680
R247B F47K
R281B 8.2K
R282B 2.2K
C282B 50V10μ
Q281B
R283B 39Ω
D282B
PC281B
PC282B
Q282B
R285B 100K
R284B 4.7K
ZR281B
R259B 1.0K
R288B 1.2K
R287B 1W22K
C283B 250V0.47μ
R286B 0.25W5.6
L281B
L283B
L282B
L284B
C284B 2200P
SA281B
SA282B
SA283B
C233B Z0.1μ
IC242B
C235B Z0.1μ
IC243B
IC244B
C237B Z0.1μ
-5VA
C272B Z0.1μ
5 TB
6 RB
7 HB
8 LB
N.C.
N.C.


CN291 PIN ASSIGNMENT
(SOLDER SIDE VIEW)
RA LA RB LB
HA TA HB TB

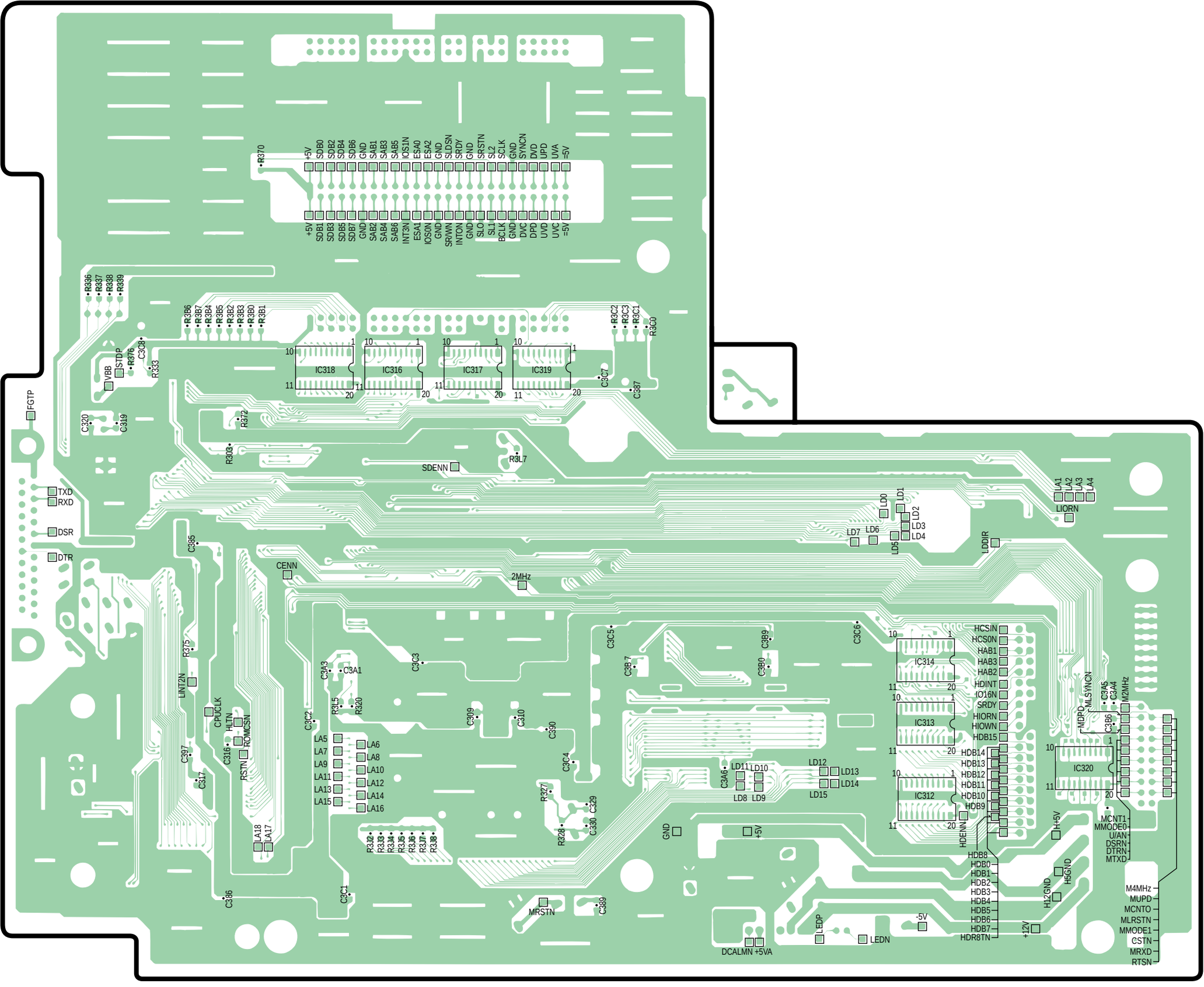

FG_Base
SA280
PQVDDSSV301Y


CN101
CN102
DC Power
Bus Buffer
Slave Controller
HOST I/F(50P)
CN101
144-FQFP
COL ASIC
IC101
Parallel DSP Port
for DSP-A accesing
the various registers
in the IC101
Parallel DSP Port
for DSP-B accesing
the various registers
in the IC101
Parallel microprocessor
Port for microprocessor
accessing the various
registers in the IC101
Rerial Voice Port
for Voice/PITS
data transfer
DSP
Serial
Port
COL I/F(30P)
CN102
CODEC
Interface
CO Line
Control
D-PITS
Interface
R106
No Mounted
R107
0
R105
47K
MODE1
R100
33
R109
No Mounted
X100
16.384MHz
R108
220Ω
C100
1000P
C101
1000P
C102
12P
C103
12P
R102
33
R103
33
L100
No Mounted
R101
33
R141
47KΩ
Q100
R110
33
R111
33
R112
33
R113
33
R114
33
C106
100P
C107
100P
C108
1000P
C109
1000P
C110
1000P
C111
1000P
C112
1000P
C113
1000P

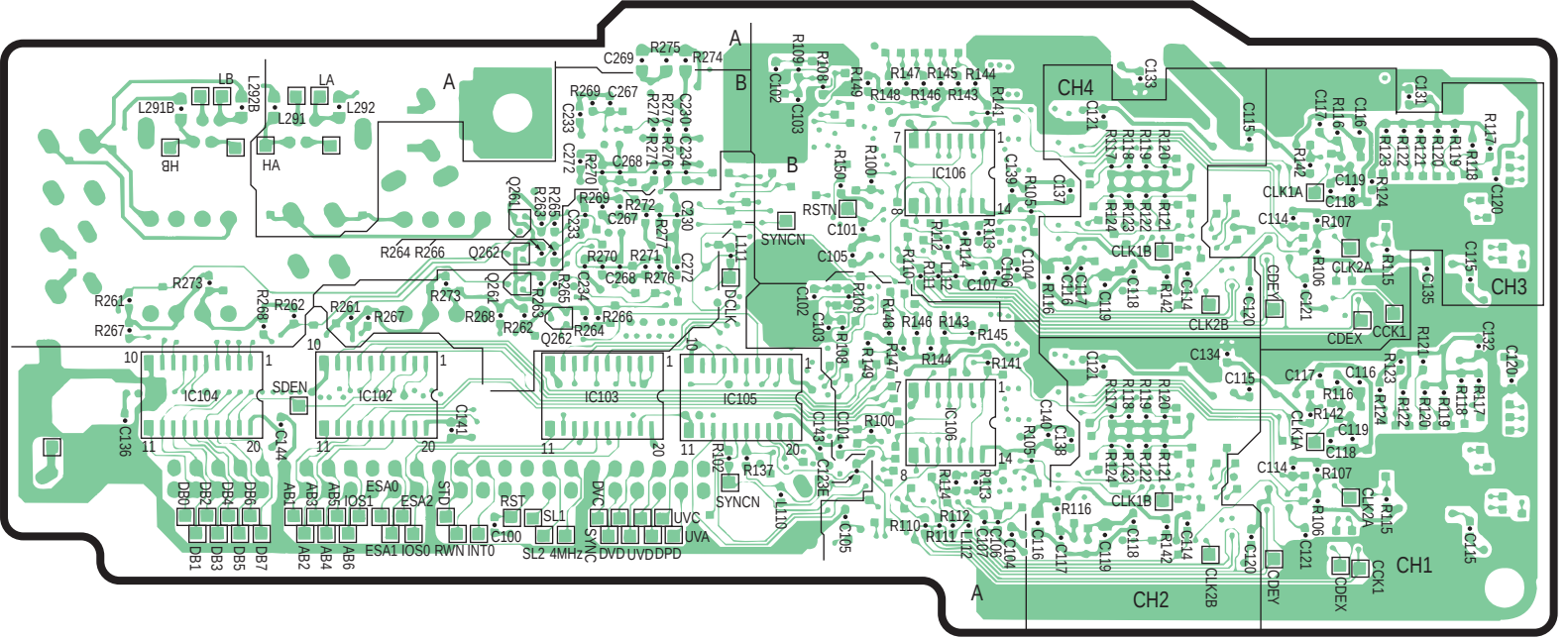

KX-TVS102 (DSP CARD)(OPTION) No.2
100-QFP
DSP LSI
IC109A
DSP
IC109B
DSP Serial Port
CODEC Port
DSP Program Rom
IC107A
IC108A
IC107B
IC108B
32-PLCC
AM27H256
LDSAN,LDSBN,LR/WAN,LR/WBN,LRSTAN,LRSTBN,LSTAAN,LSTBBN,MP/MCN,PSAN,PSBN
DPD,UPD,ADINA,ADINB,CCK[1],CDE-X,CDE-Y,CLKA,CLKB,DIGLA,DIGLB,DIGSA,DIGSB
(1)
(2) (3) (4)
VDD
47K
2.7K
390P
1000P
0.022µ
1.0µ
Z0.1µ



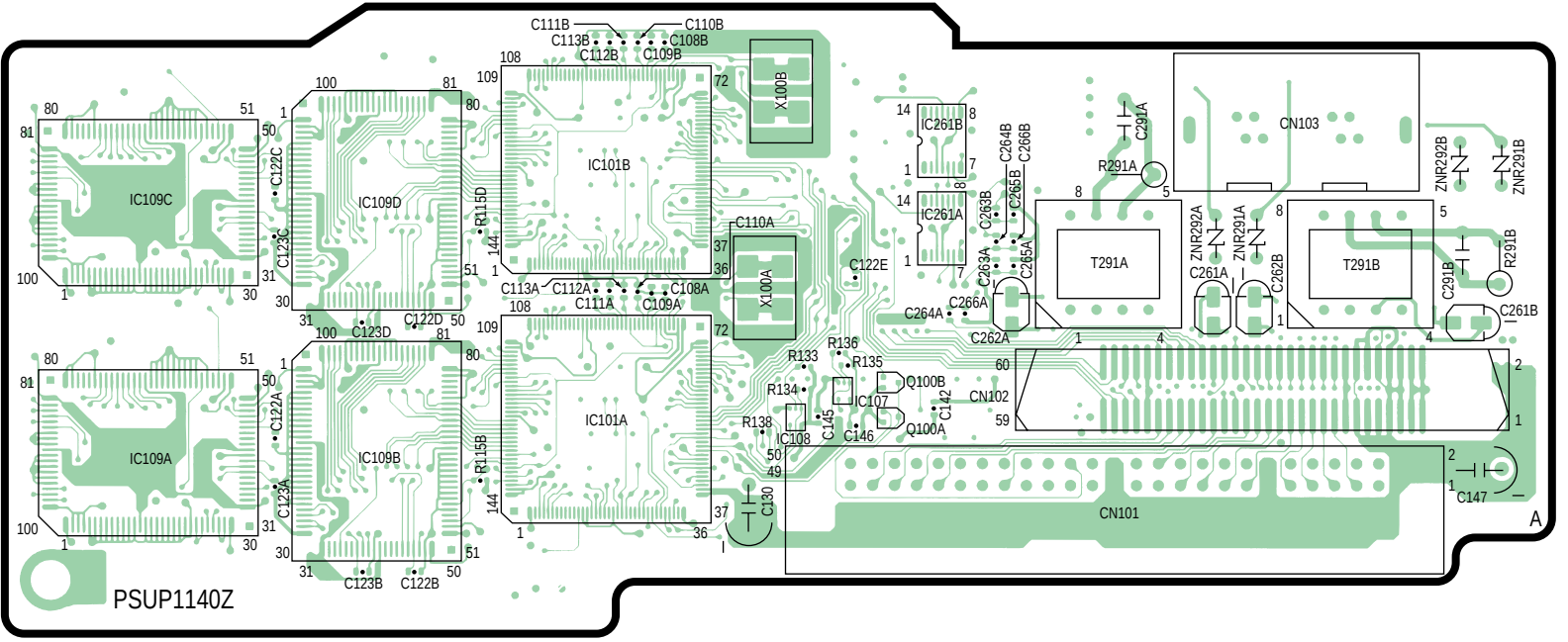
KX-TVS120 MAIN BOARD COMPONENT VIEW


R370
+5V SDB0 SDB2 SDB4 SDB6 GND SAB1 SAB3 SAB5 IOS1N ESA0 ESA2 GND SLDSN SRDY GND SRSTN SL2 SCLK GND SYNCN DVD UPD UVA =5V
+5V SDB1 SDB3 SDB5 SDB7 GND SAB2 SAB4 SAB6 INT3N ESA1 IOS0N GND SR/WN INTON GND SLO SL1 BCLK GND DVC DPD UVD UVC =5V
R336 R337 R338 R339
R3B6 R3B7 R3B4 R3B5 R3B2 R3B3 R3B0 R3B1
R3C2 R3C3 R3C1 R3C0
IC318 IC316 IC317 IC319
C3C8 R376 STDP VBB R333
C3C7 C387
FGTP
C320 C319 R372 R308
SDENN R3L7
TXD RXD DSR DTR
C385
CENN
2MHz
LD0 LD1 LD2 LD3 LD4 LD5 LD6 LD7
LA1 LA2 LA3 LA4 LIORN
LDDIR
C3C5 C3B7 C3B9 C3B0 C3C6
IC314 IC313 IC312
HCSIN HCS0N HAB1 HAB3 HAB2 HDINT IO16N SRDY HIORN HIOWN HDB15 HDB14 HDB13 HDB12 HDB11 HDB10 HDB9 HDENN
IC320
MDPD MLSYNCN C3A5 C3A4 M2MHz C3B6
MCNT1 MMODE0 U/AN DSRN DTRN MTXD
M4MHz MUPD MCNTO MLRSTN MMODE1 CSTN MRXD RTSN
H+5V H5GND H12GND +12V
HDB8 HDB0 HDB1 HDB2 HDB3 HDB4 HDB5 HDB6 HDB7 HDR8TN
R375 LINT2N
C3A3 C3A1 C3C3
R315 R320
C3C2
CPUCLK HLTN ROMCSN RSTN
C397 C316 C317
LA5 LA7 LA9 LA11 LA13 LA15 LA6 LA8 LA10 LA12 LA14 LA16
LA18 LA17
C309 C310 C390 C3C4
C3A6 LD11 LD10 LD8 LD9 LD12 LD13 LD14 LD15
R327 R328 C330 C329
R332 R333 R334 R335 R336 R337 R338
GND +5V
C3C1 C386
MRSTN C389
DCALMN +5VA
LEDP LEDN -5V

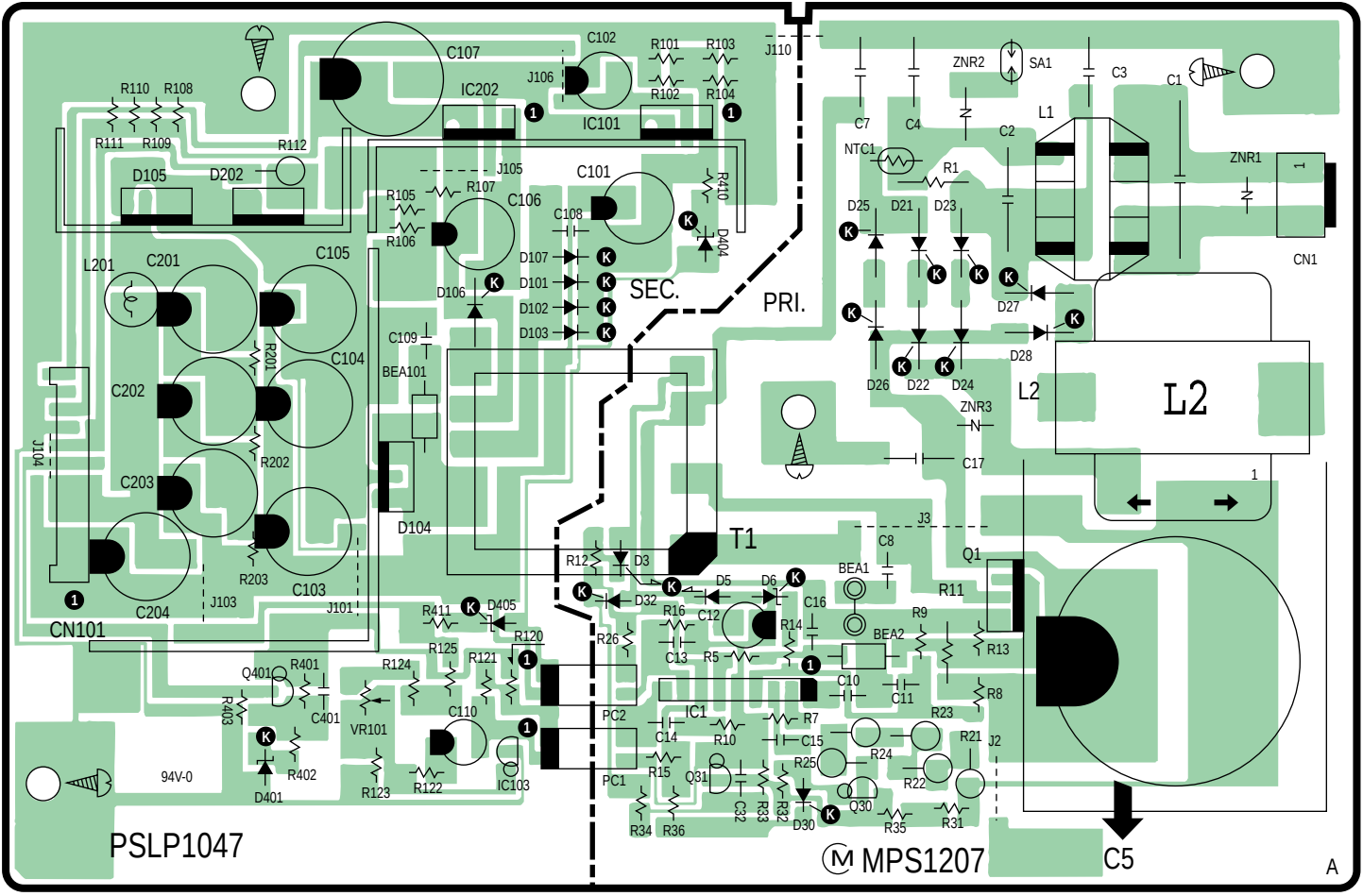
KX-TVS120 MAIN BOARD BOTTOM VIEW



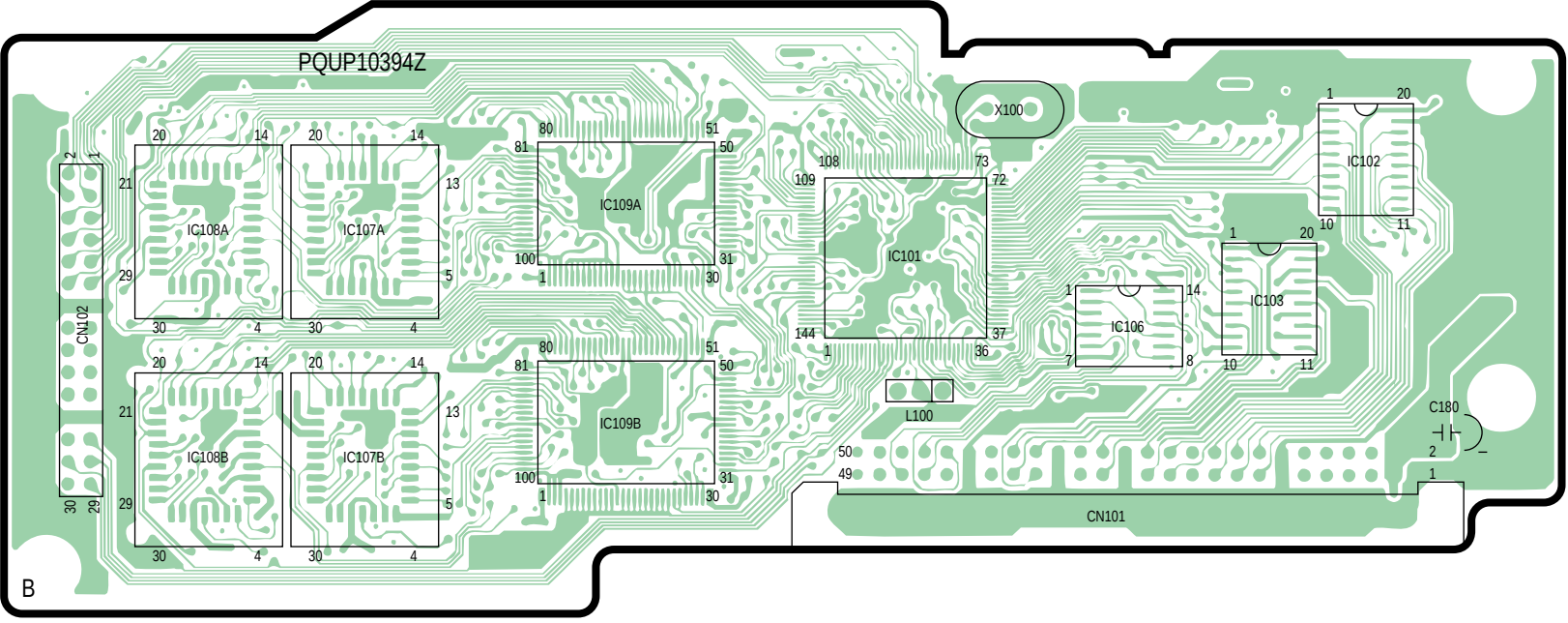
KX-TVS120 DPT INTERFACE CARD(KX-TVS204) COMPONENT VIEW



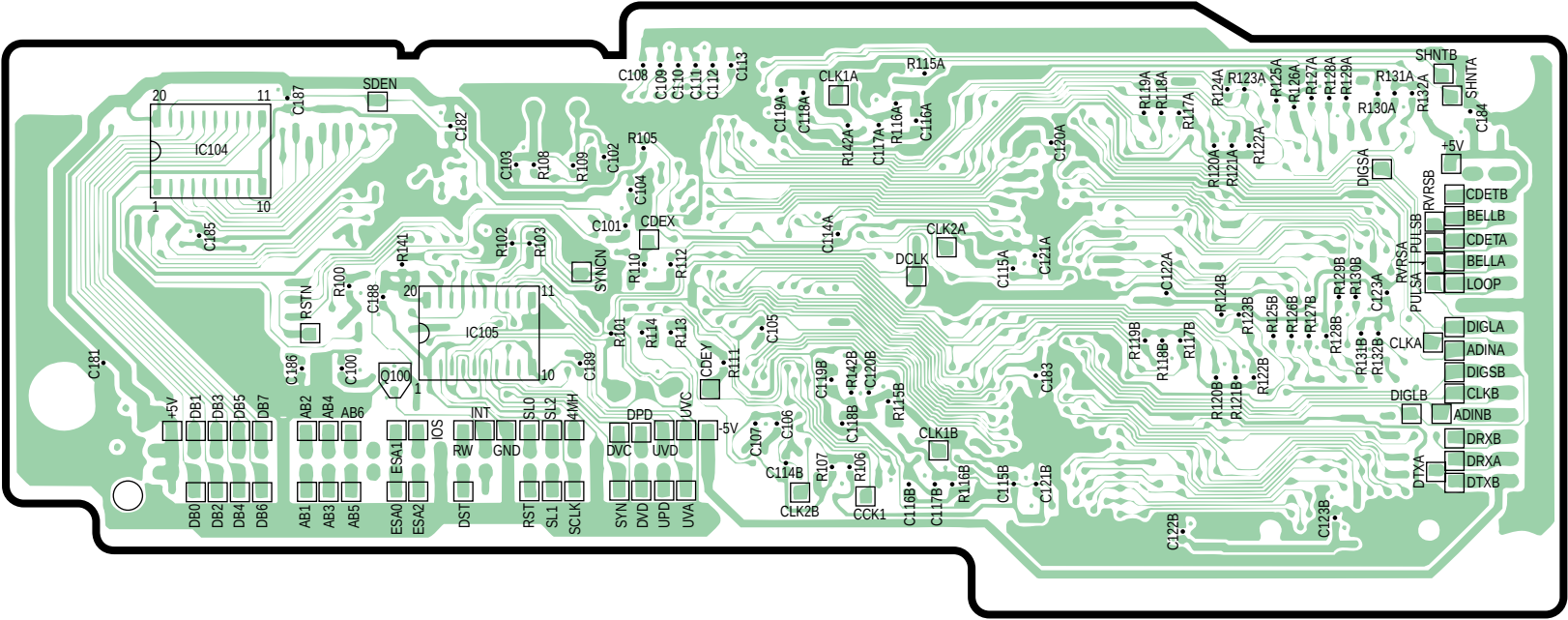
KX-TVS120 DPT INTERFACE CARD(KX-TVS204) BOTTOM VIEW



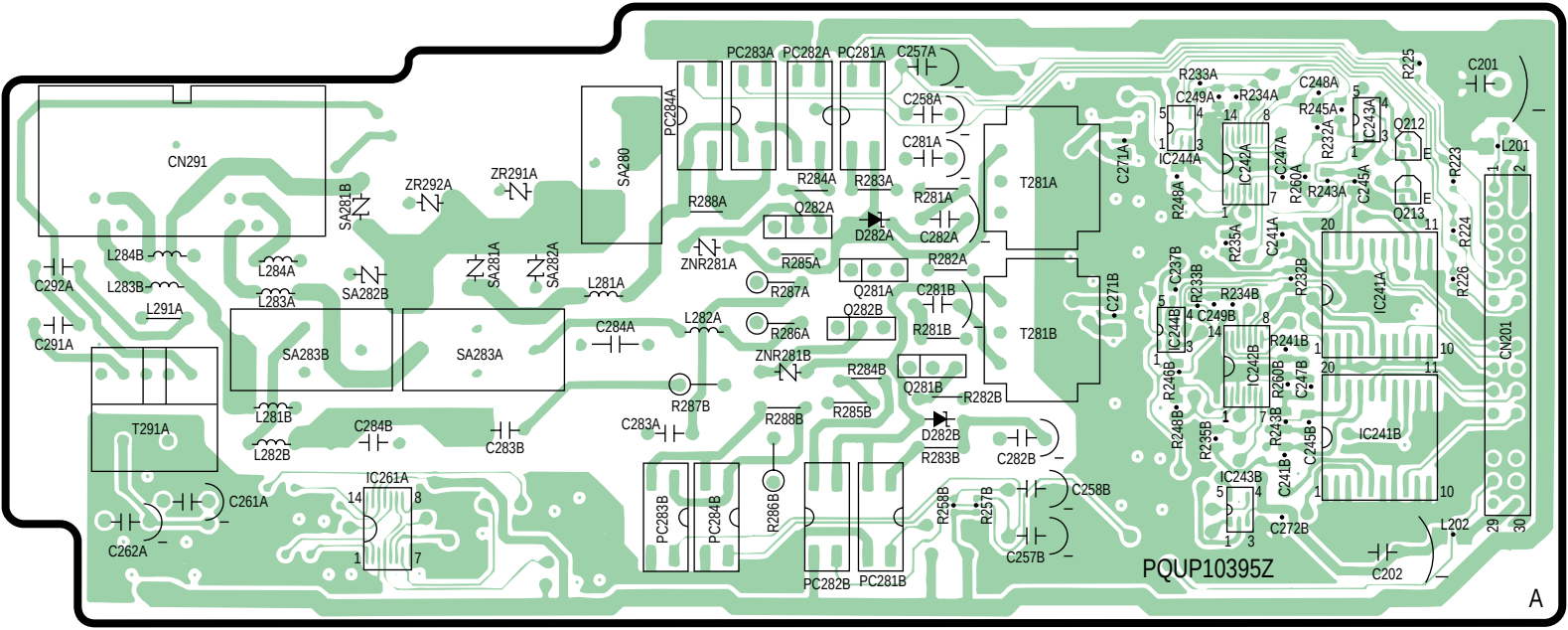
KX-TVS120 POWER SUPPLY BOARD



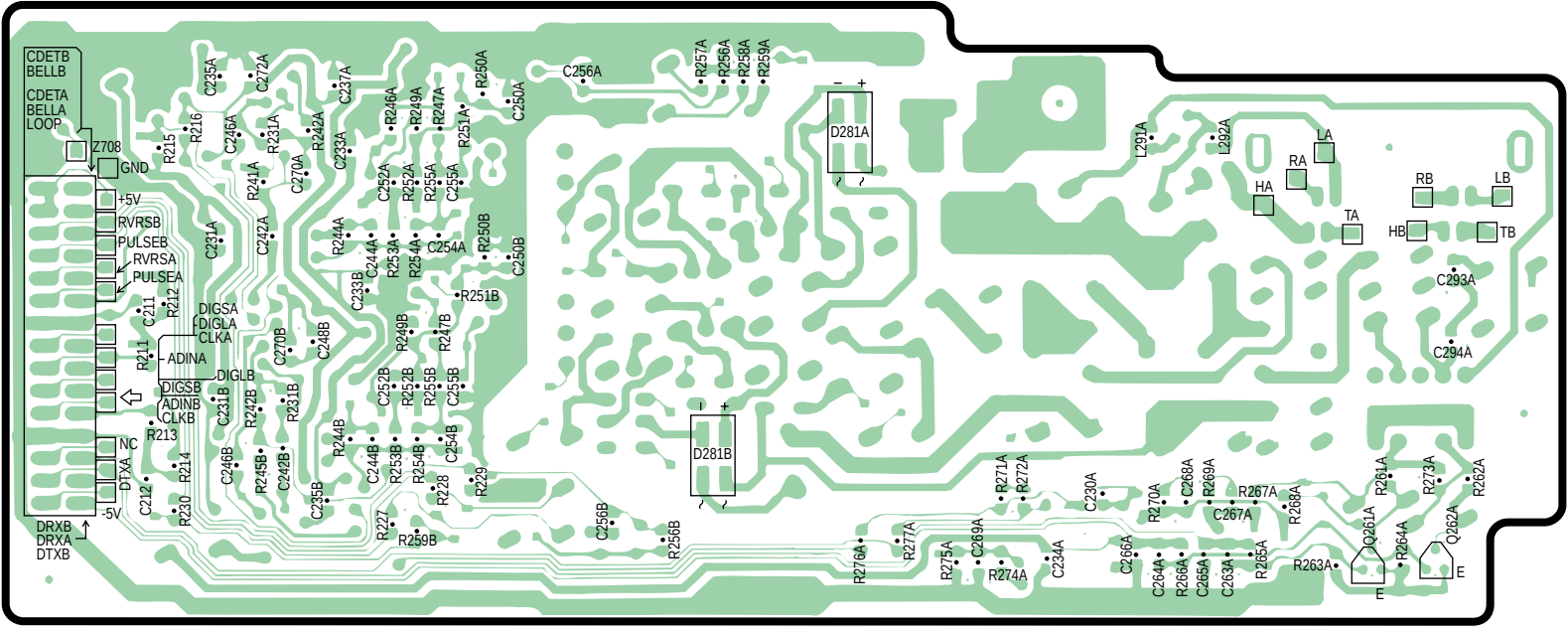
KX-TVS102(DSP CARD)(OPTION) COMPONENT VIEW



KX-TVS102(DSP CARD)(OPTION) BOTTOM VIEW



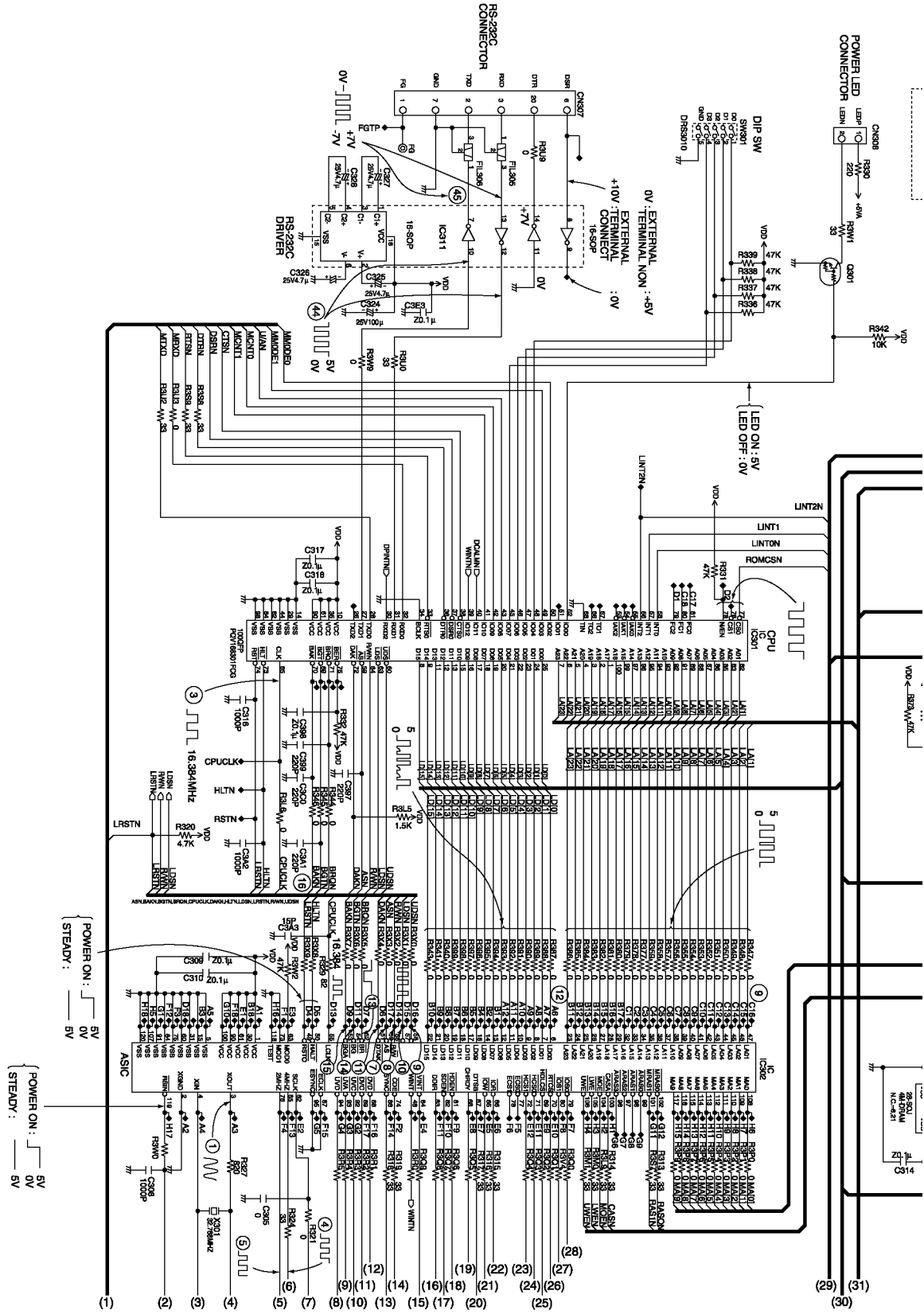
KX-TVS102 (CO CARD)(OPTION) COMPONENT VIEW

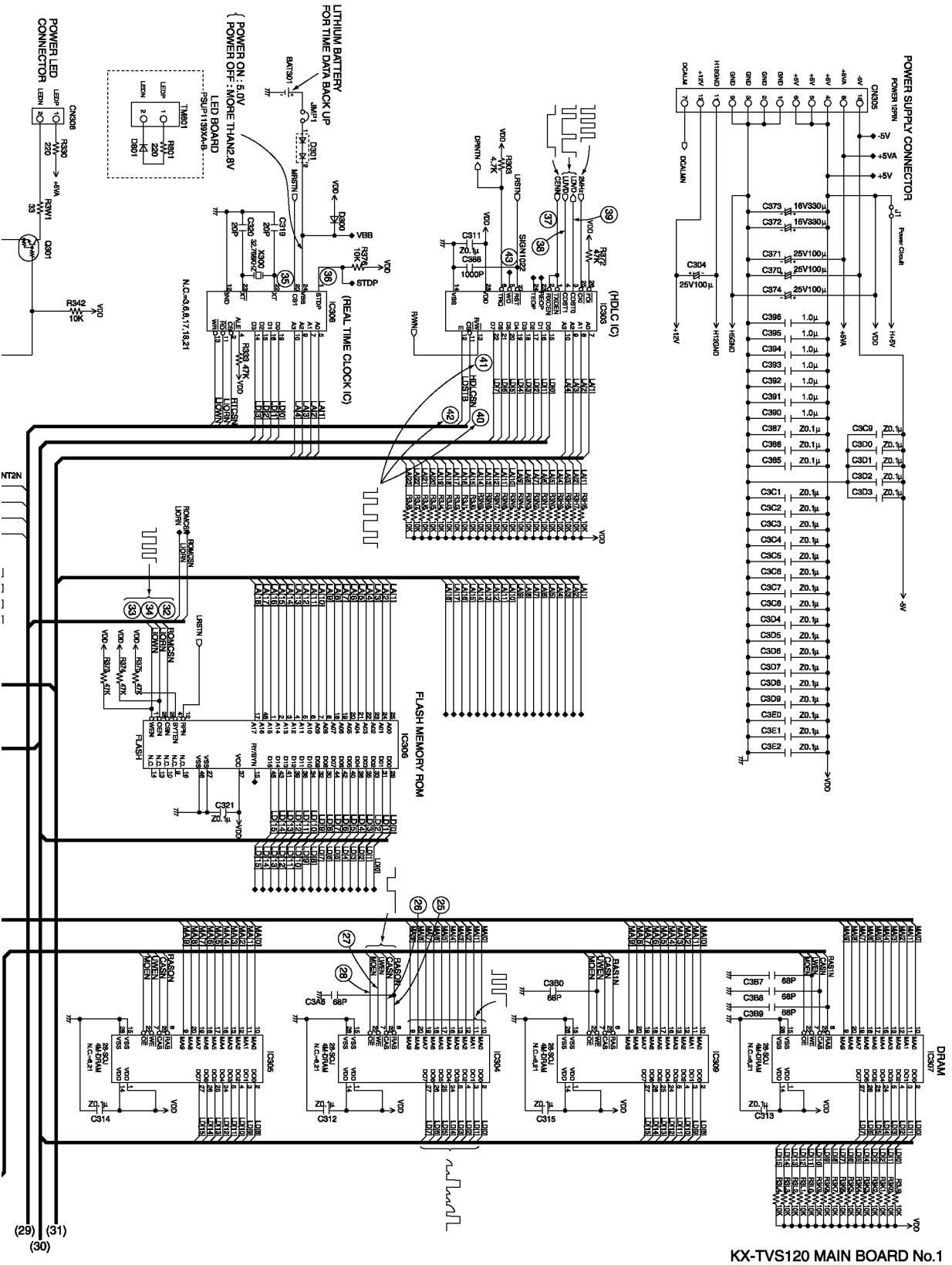


KX-TVS102 (CO CARD)(OPTION) BOTTOM VIEW

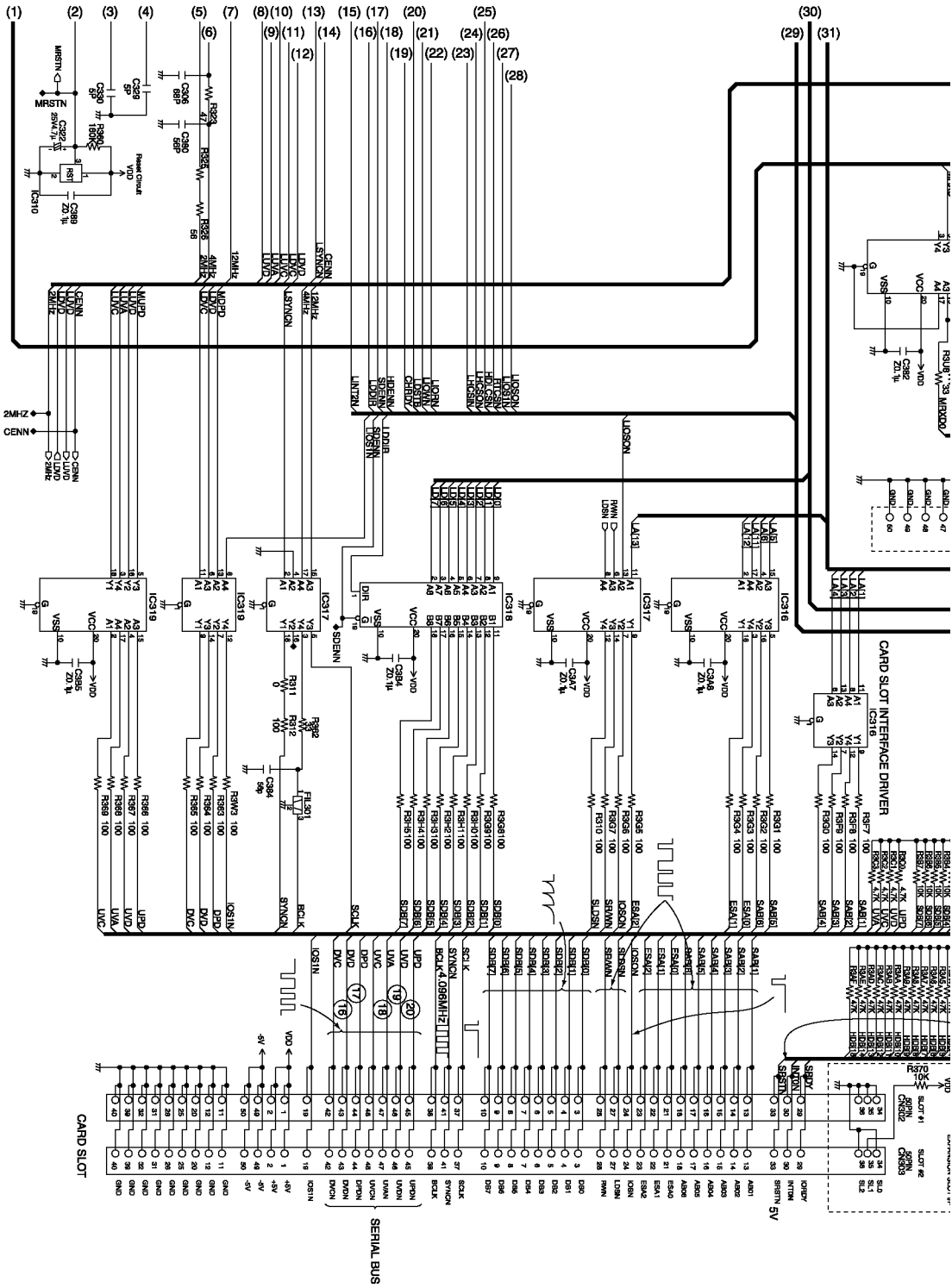
22 SCHEMATIC DIAGRAM

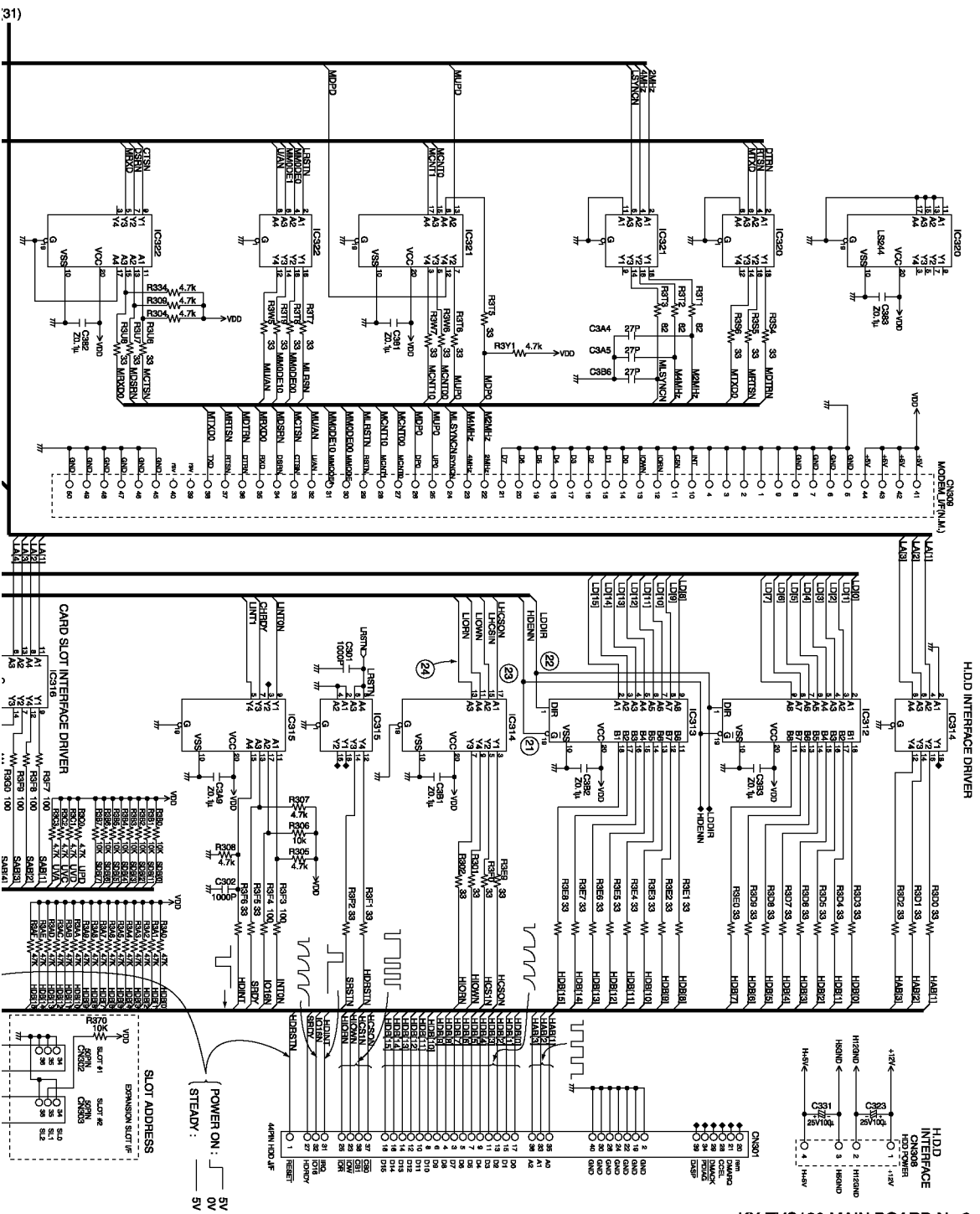
22.1. MAIN BOARD





KX-TVS120 MAIN BOARD No.1

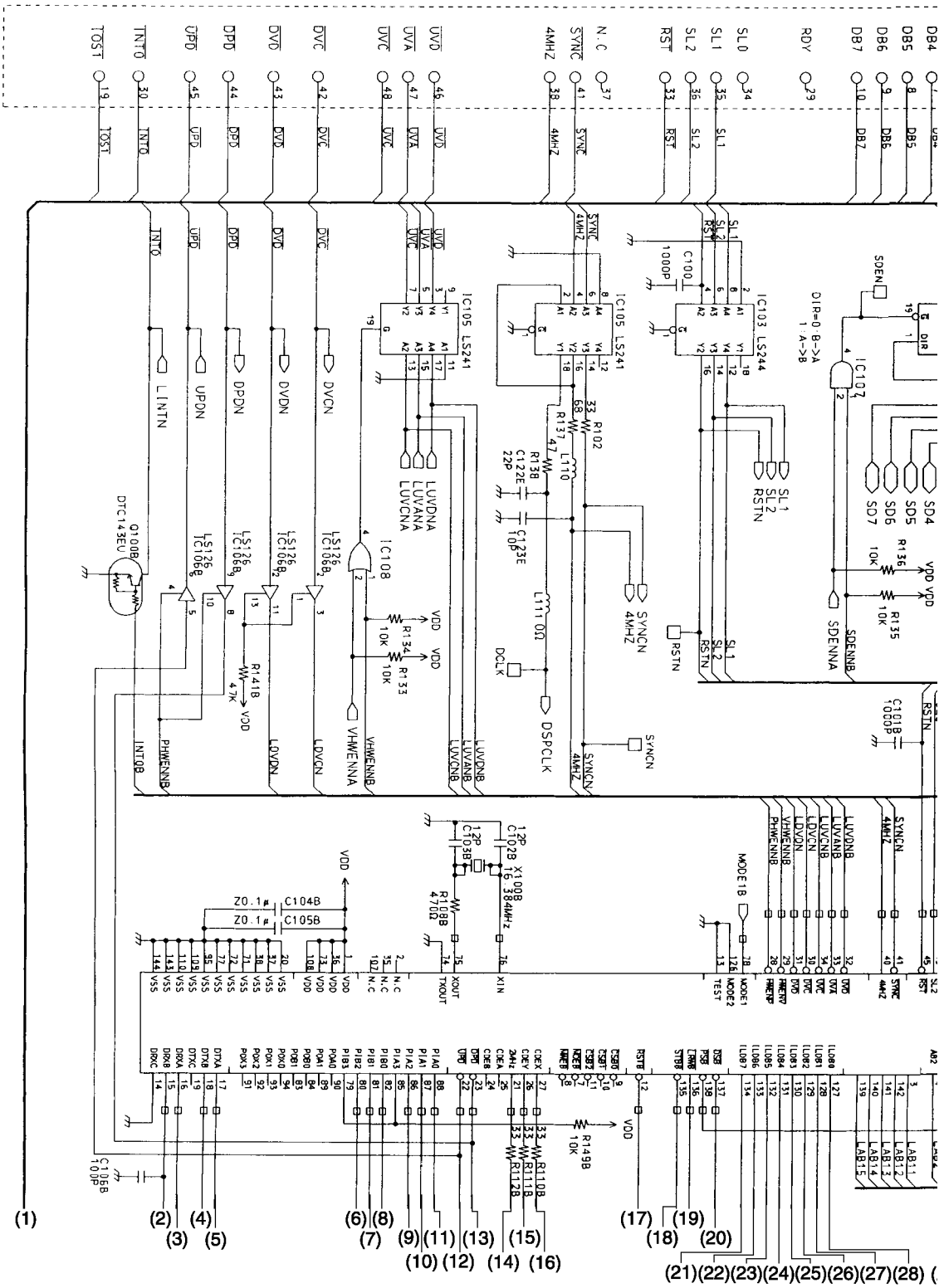

CARD SLOT INTERFACE DRIVER
IC316
CARD SLOT
SERIAL BUS
MRSTN
2MHZ
CENN
5V
SLOT #1
SLOT #2
CN202
CN203

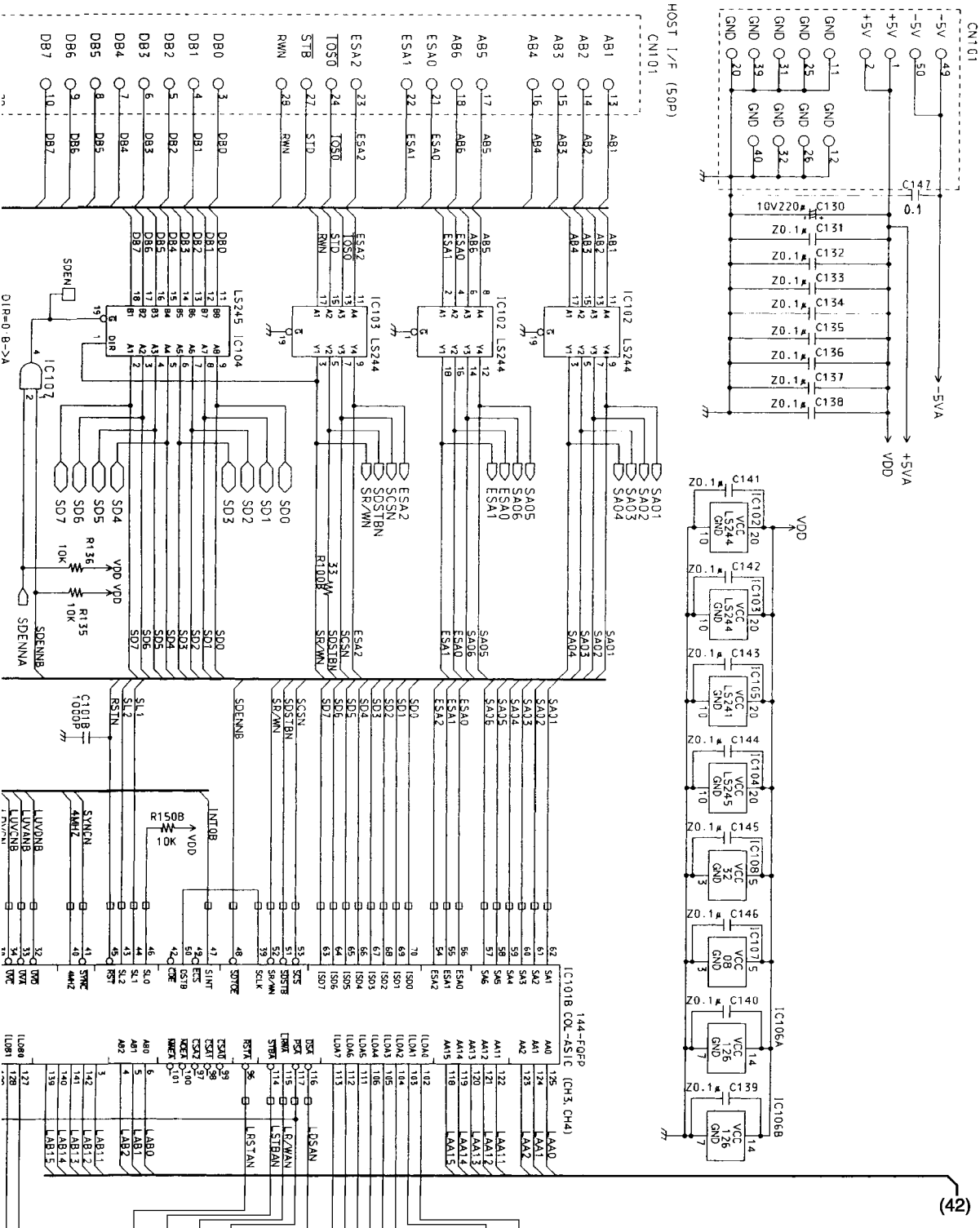


KX-TVS120 MAIN BOARD No.2

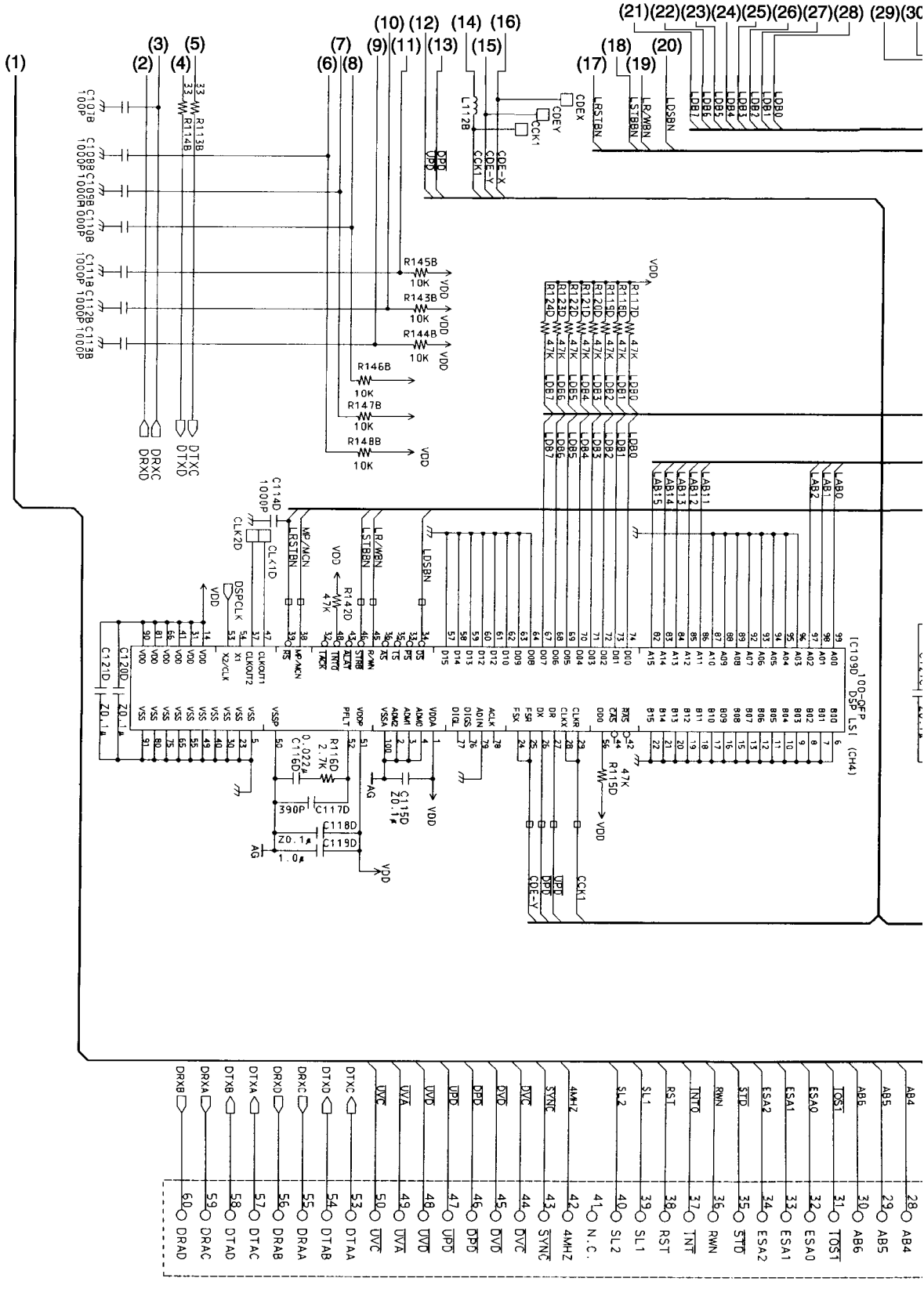
22.2. DPT INTERFACE CARD(KX-TVS204)

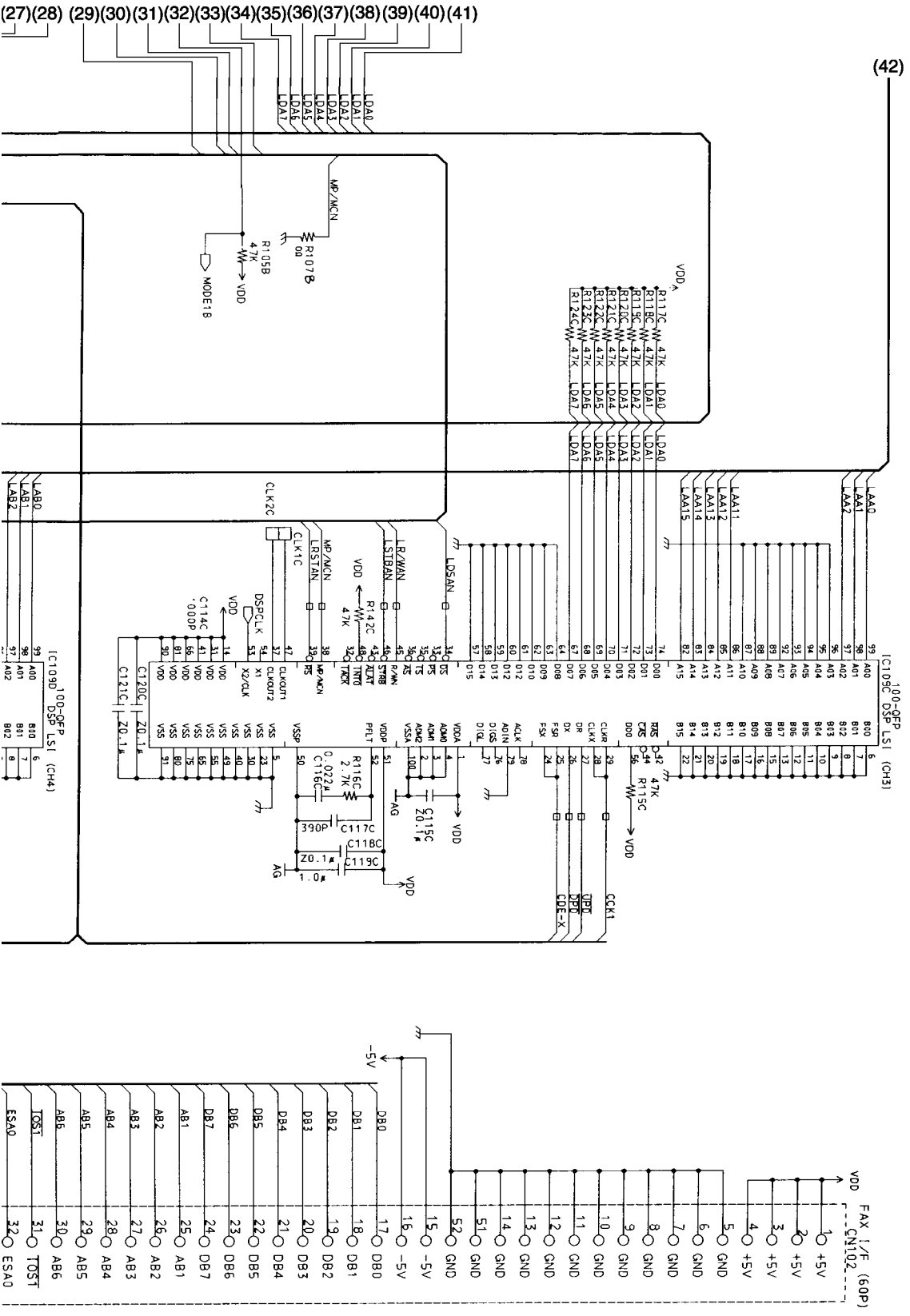
22.2.1. DPT INTERFACE CARD(KX-TVS204)(NO.1,NO.2)





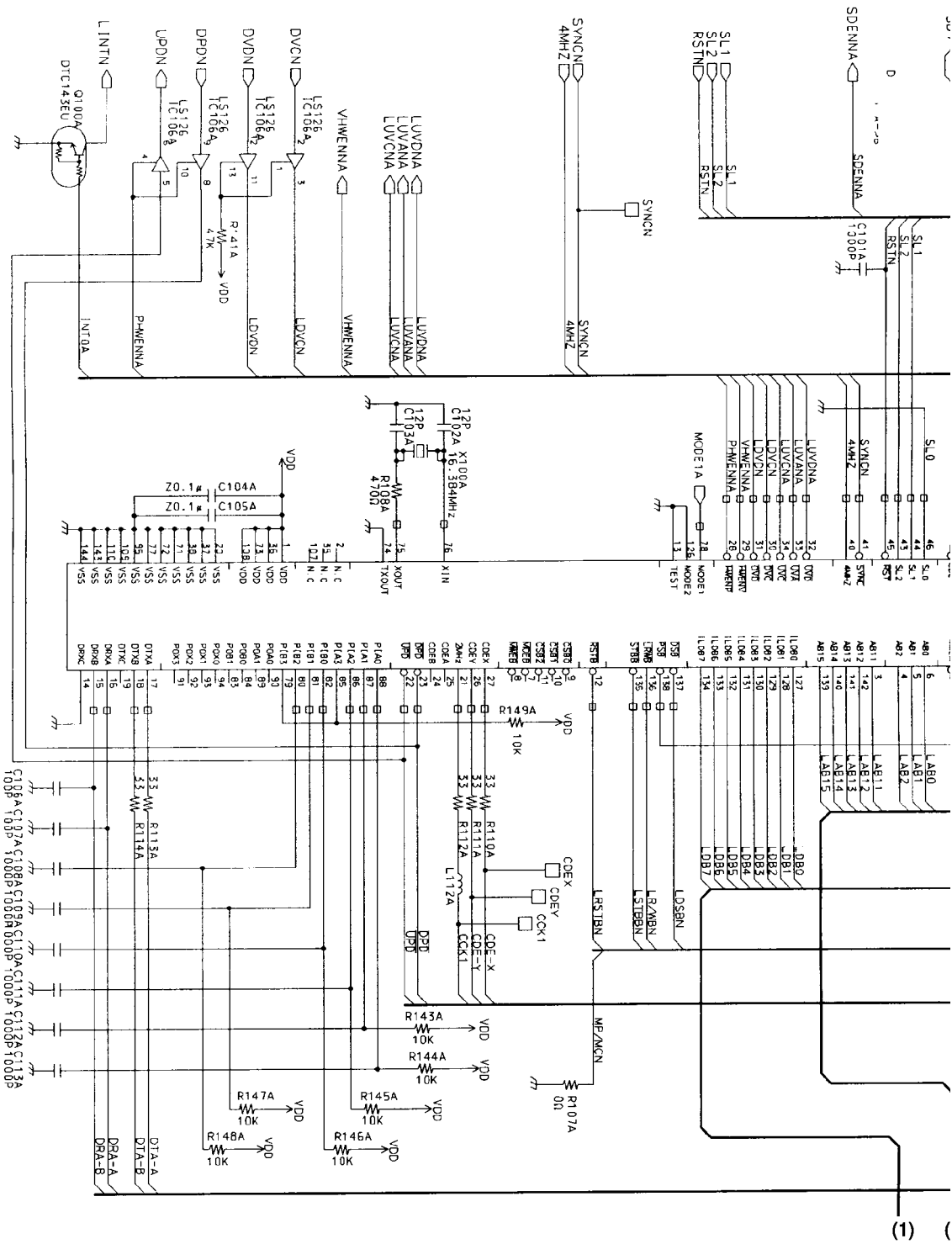
KX-TVS120 DPT INTERFACE CARD(KX-TVS204) No.1

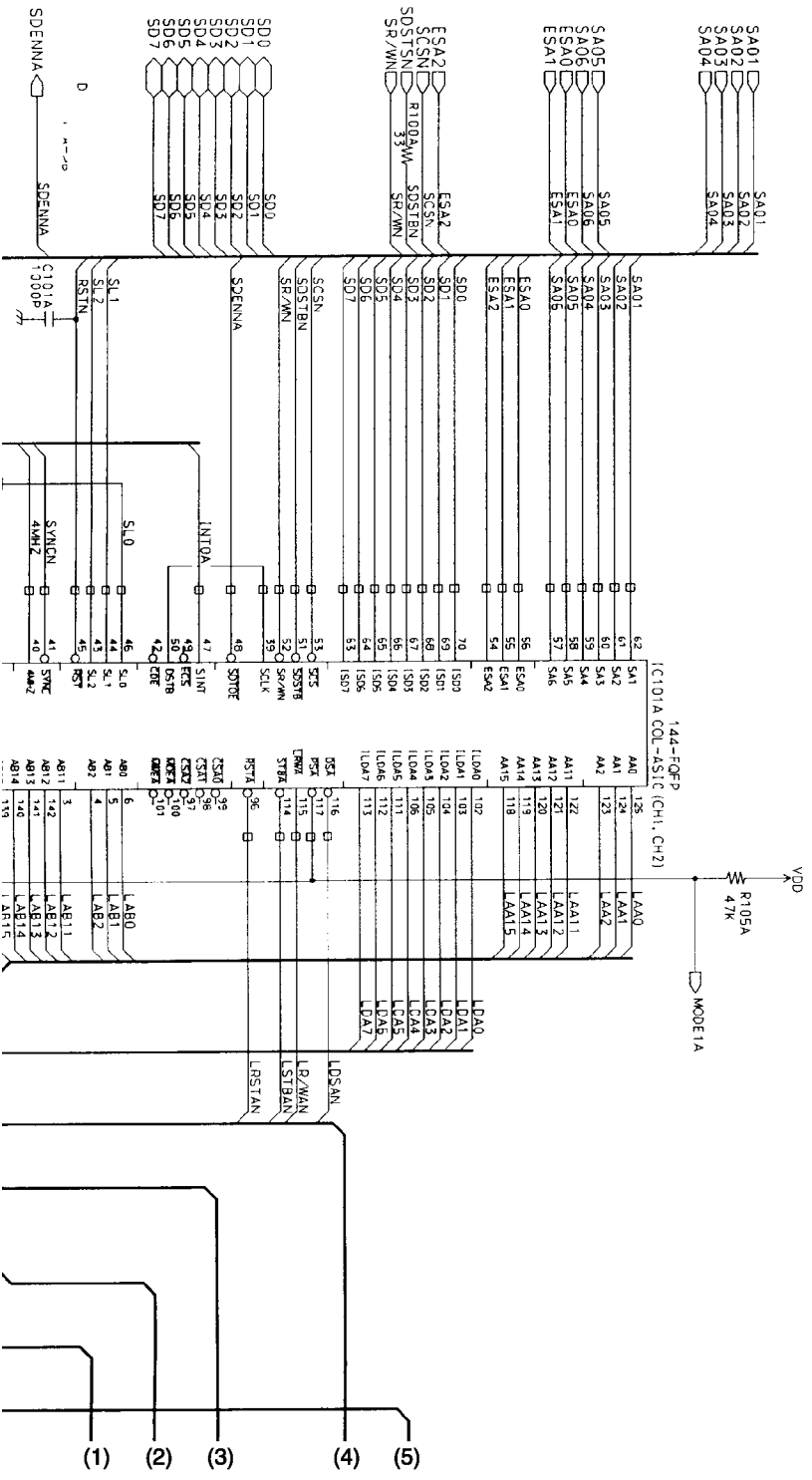




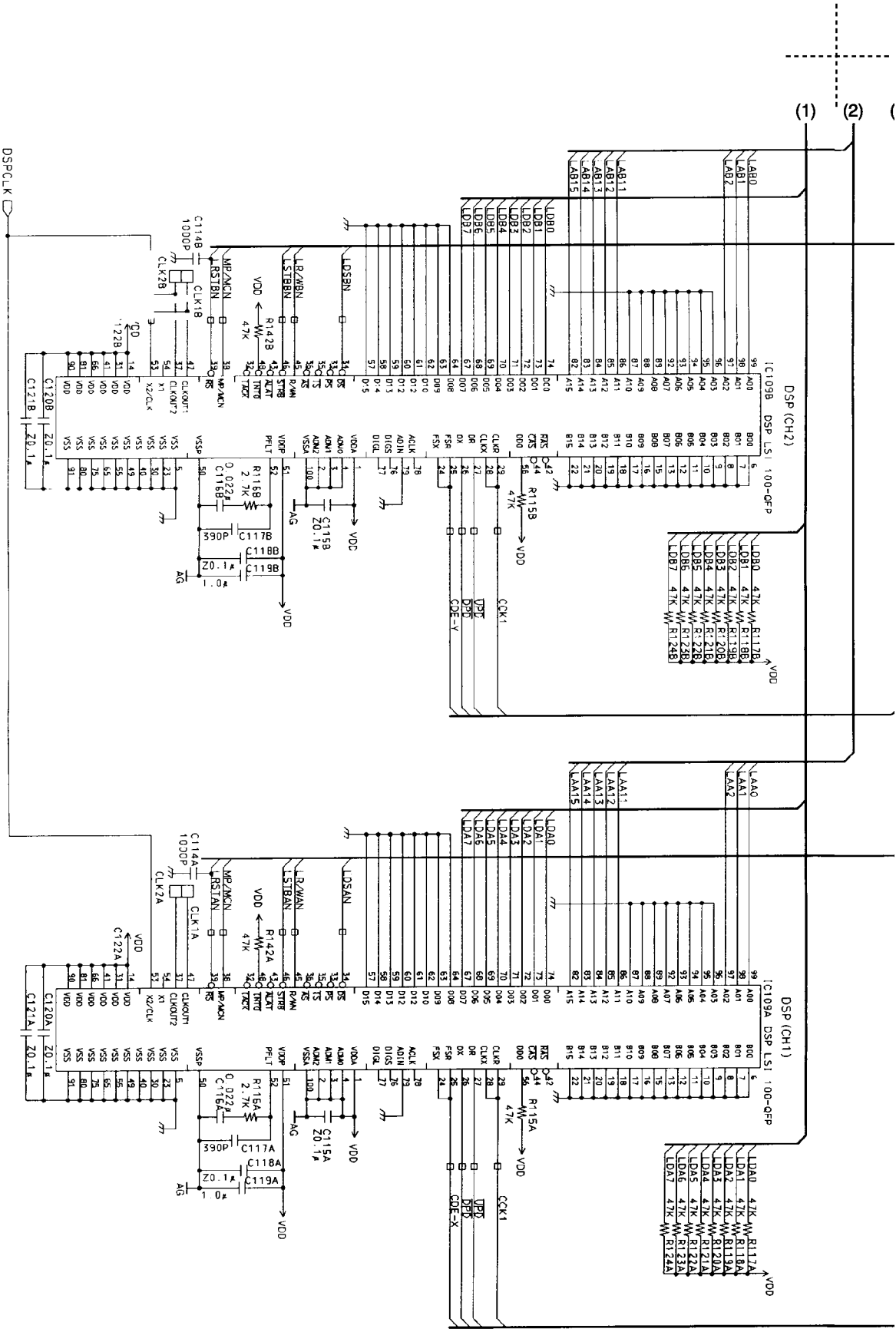
KX-TVS120 DPT INTERFACE CARD(KX-TVS204) No.2

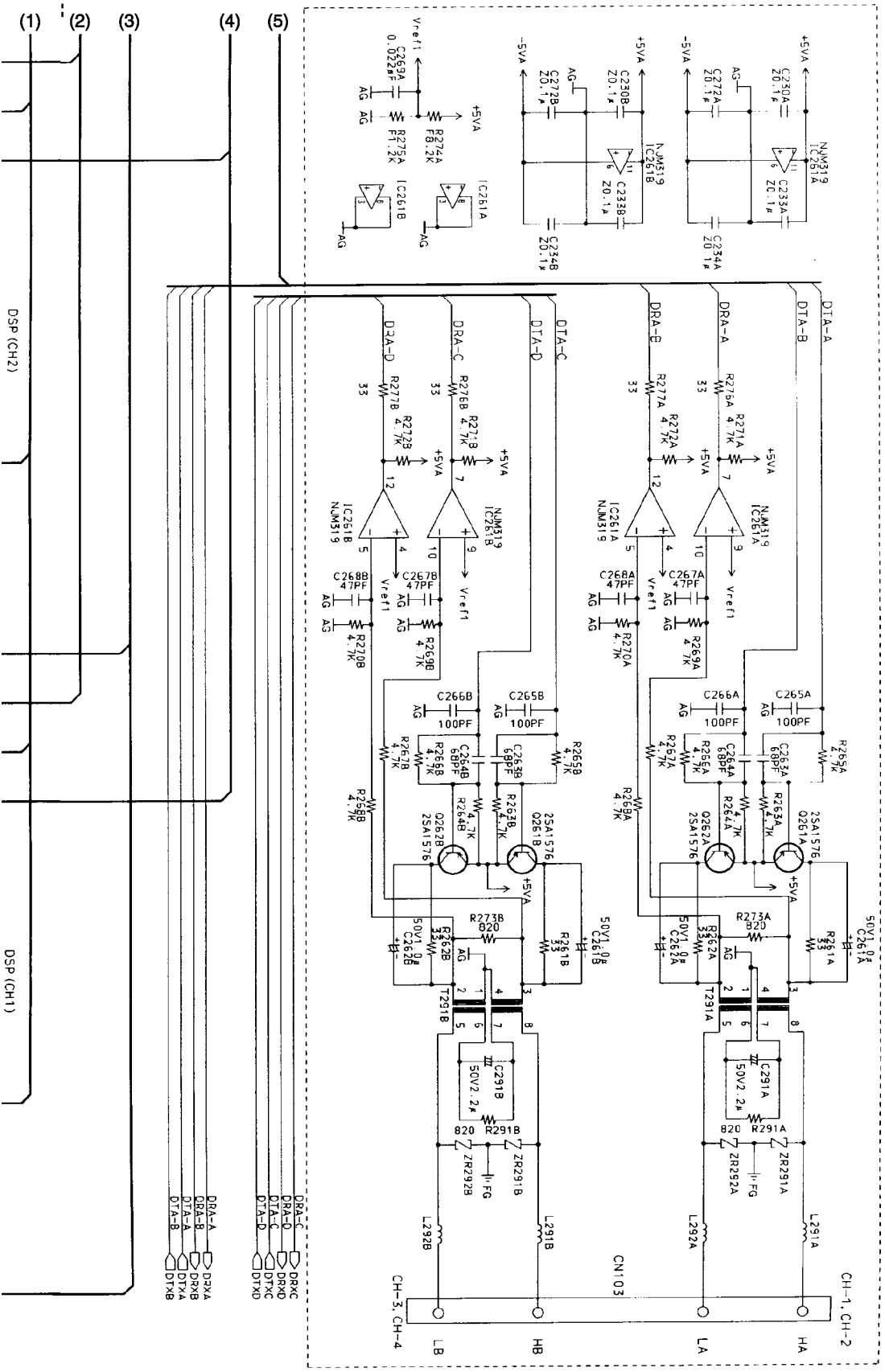
22.2.2. DPT INTERFACE CARD(KX-TVS204)(NO.3,NO.4)





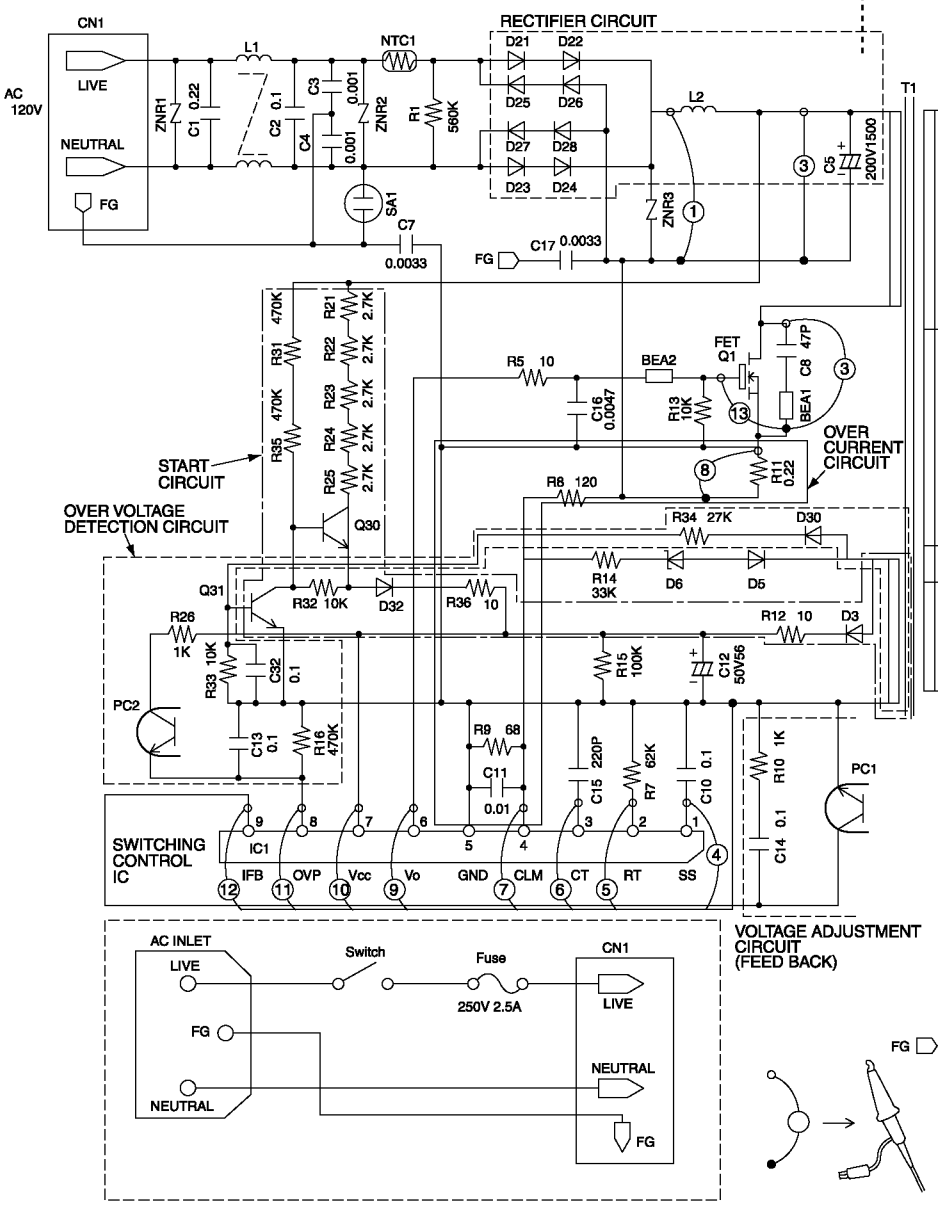
KX-TVS120 DPT INTERFACE CARD(KX-TVS204) No.3

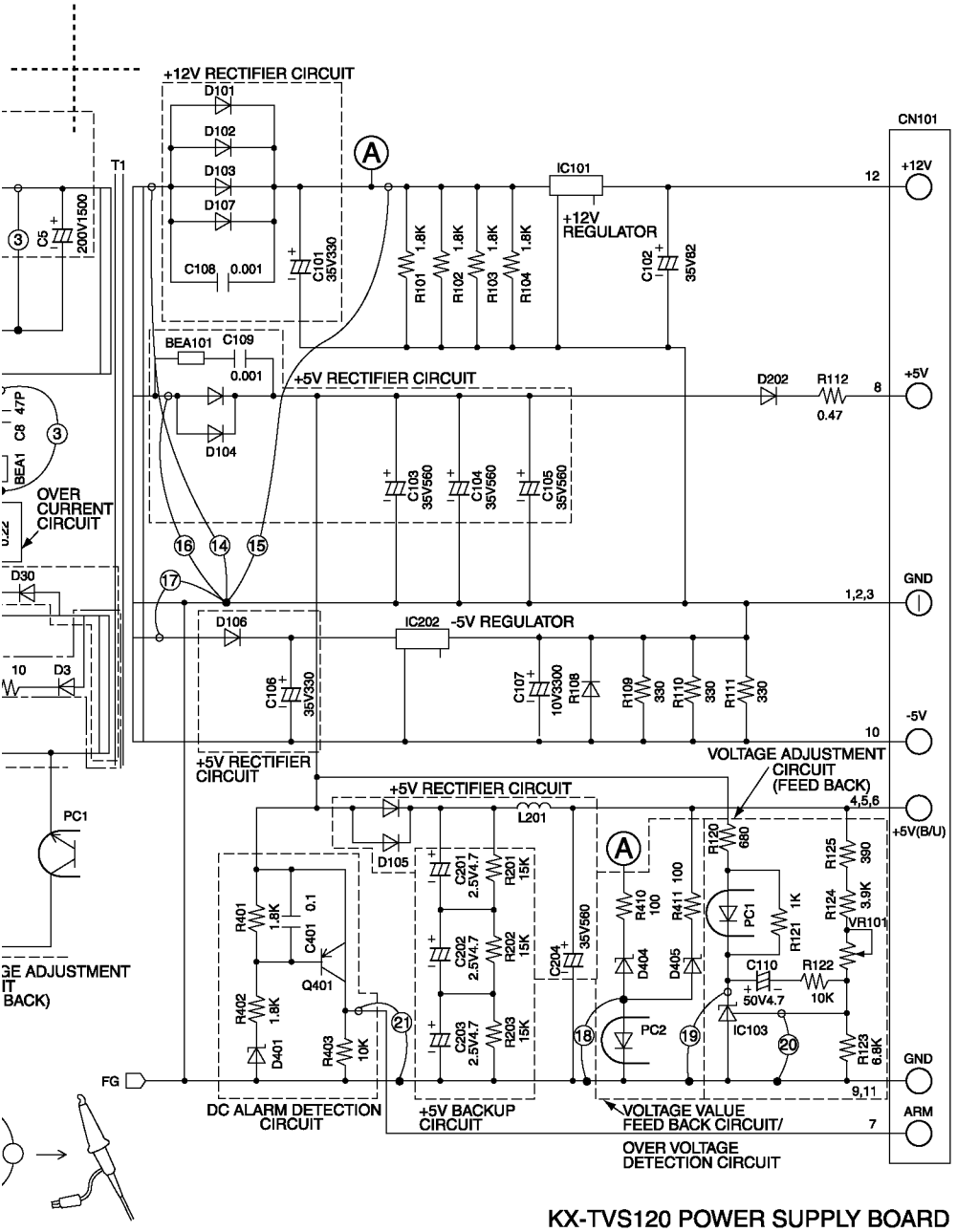

(1)
(2)
DSP (CH2)
DSP (CH1)
DSPCLK
VDD
AG
CCK1
CDE-Y
CDE-X



KX-TVS120 DPT INTERFACE CARD(KX-TVS204) No.4

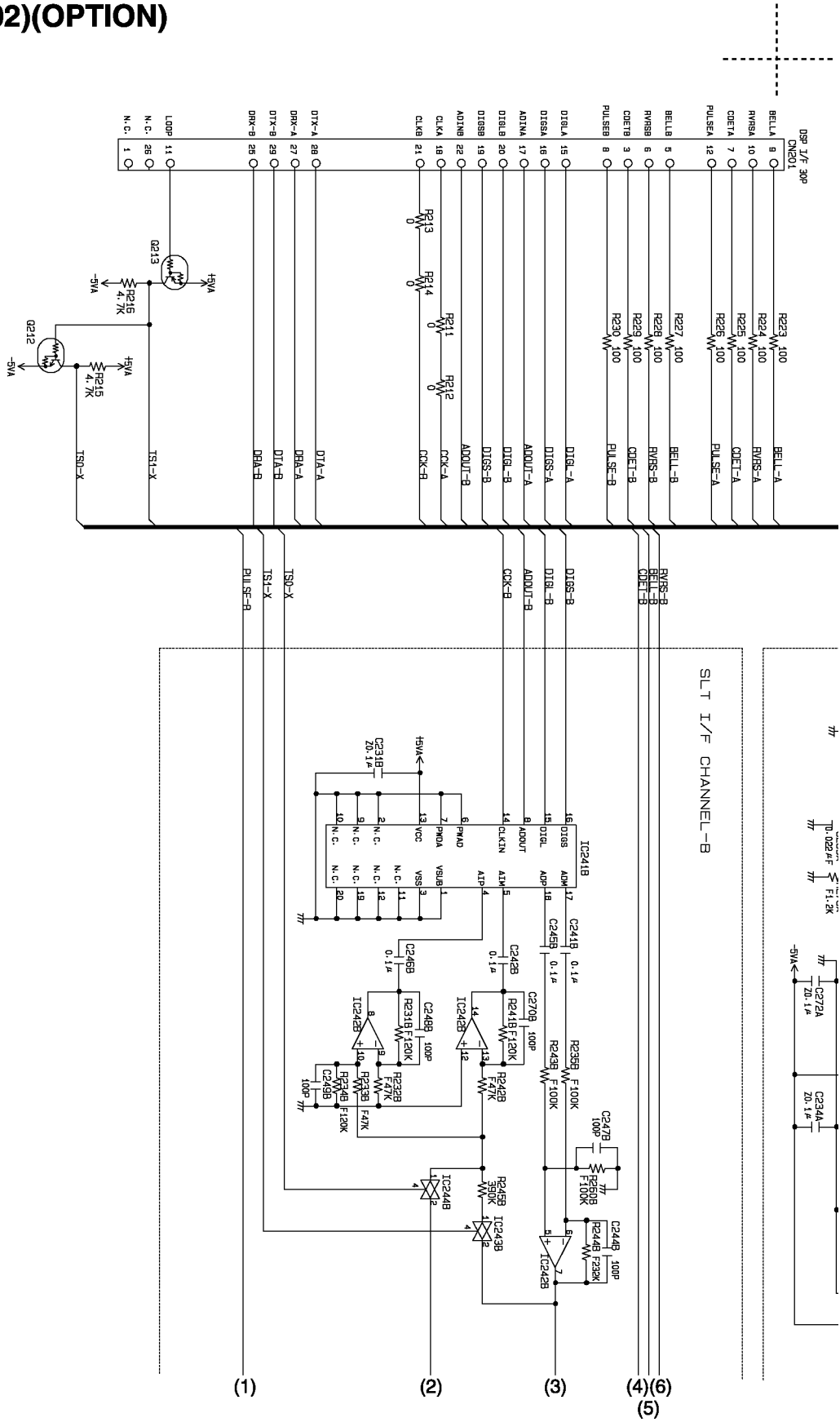
22.3. POWER SUPPLY BOARD

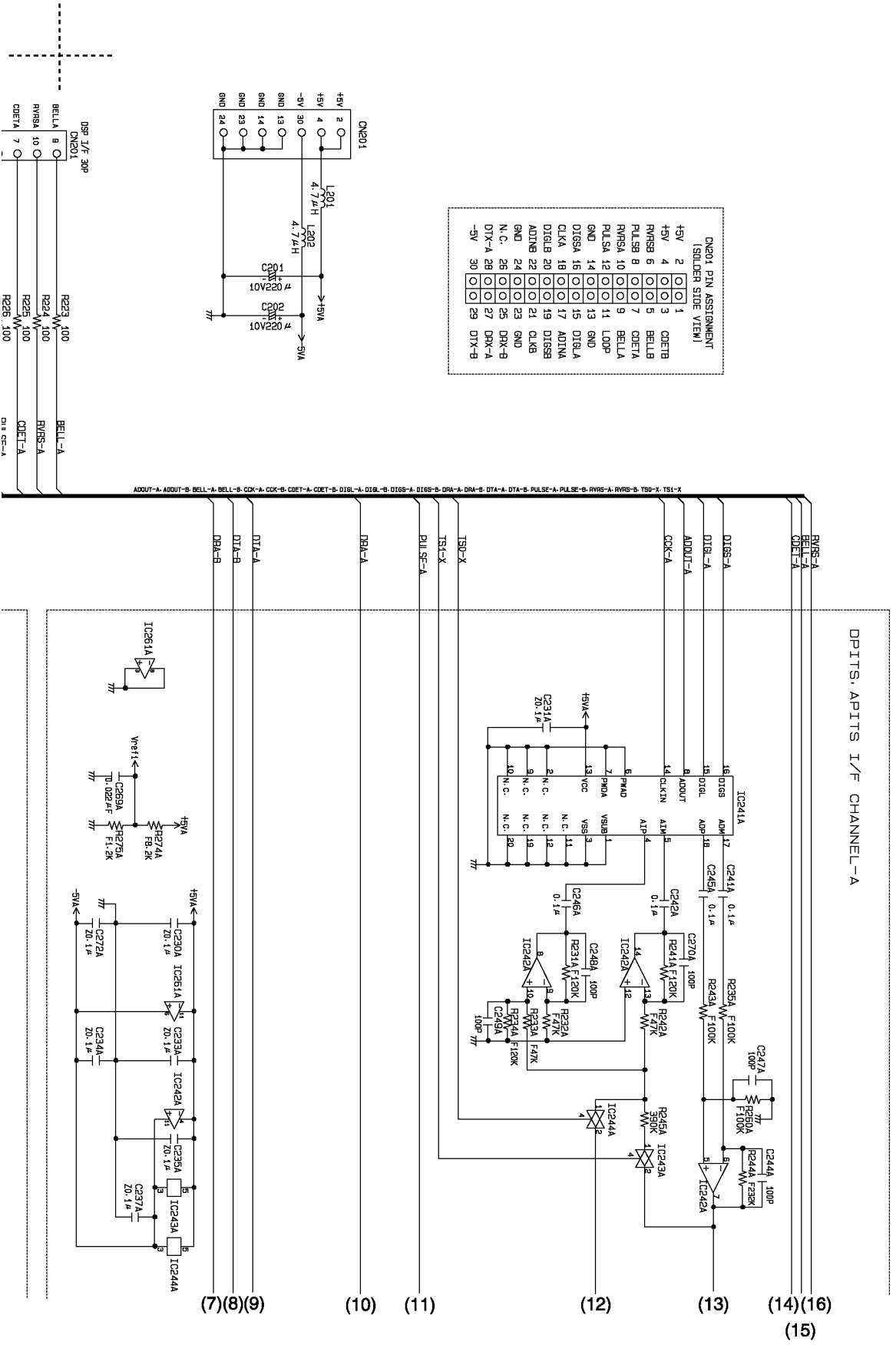


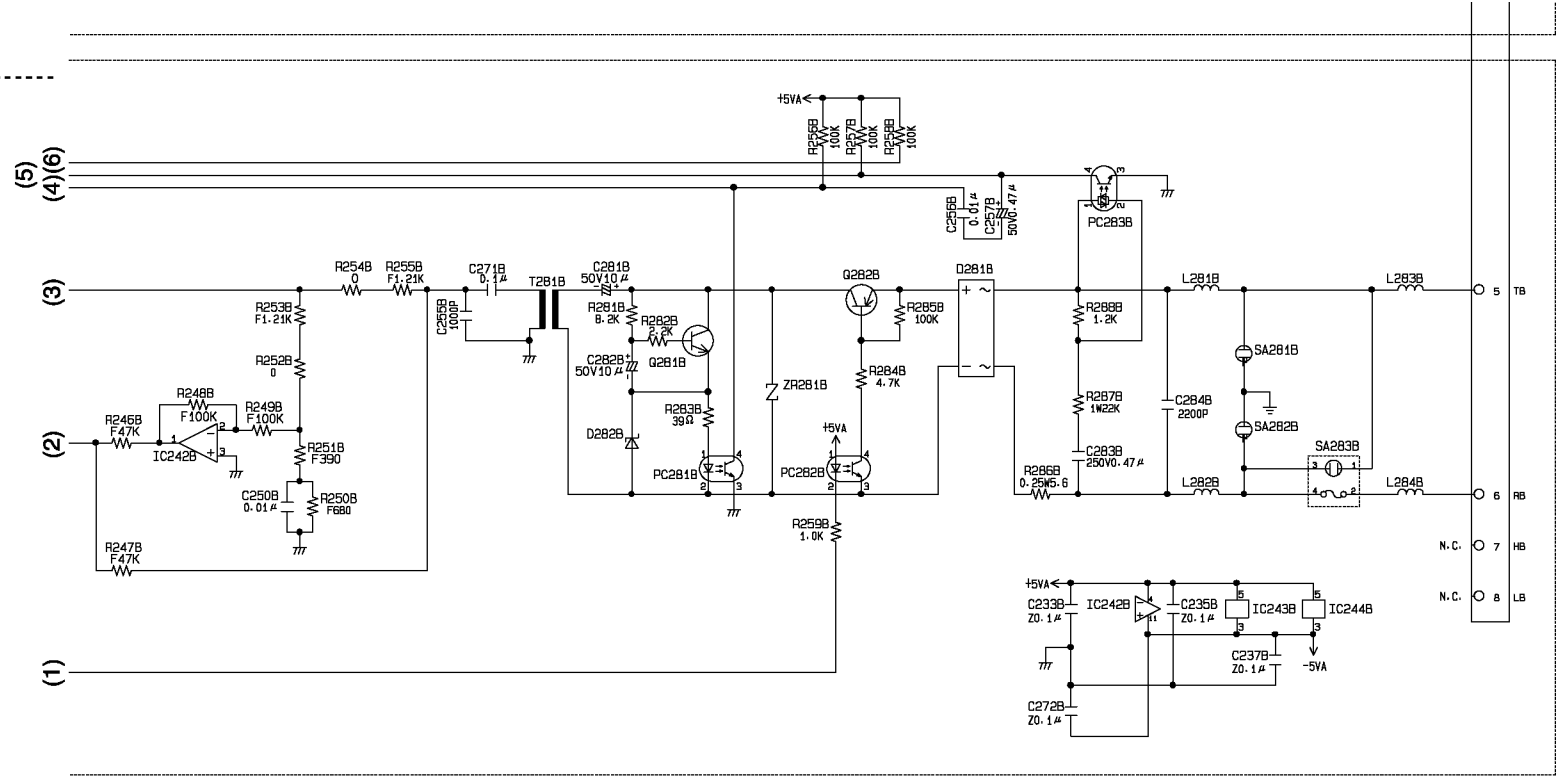


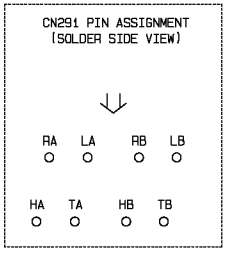
KX-TVS120 POWER SUPPLY BOARD

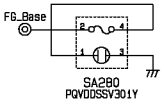
22.4. CO CARD (KX-TVS102)(OPTION)

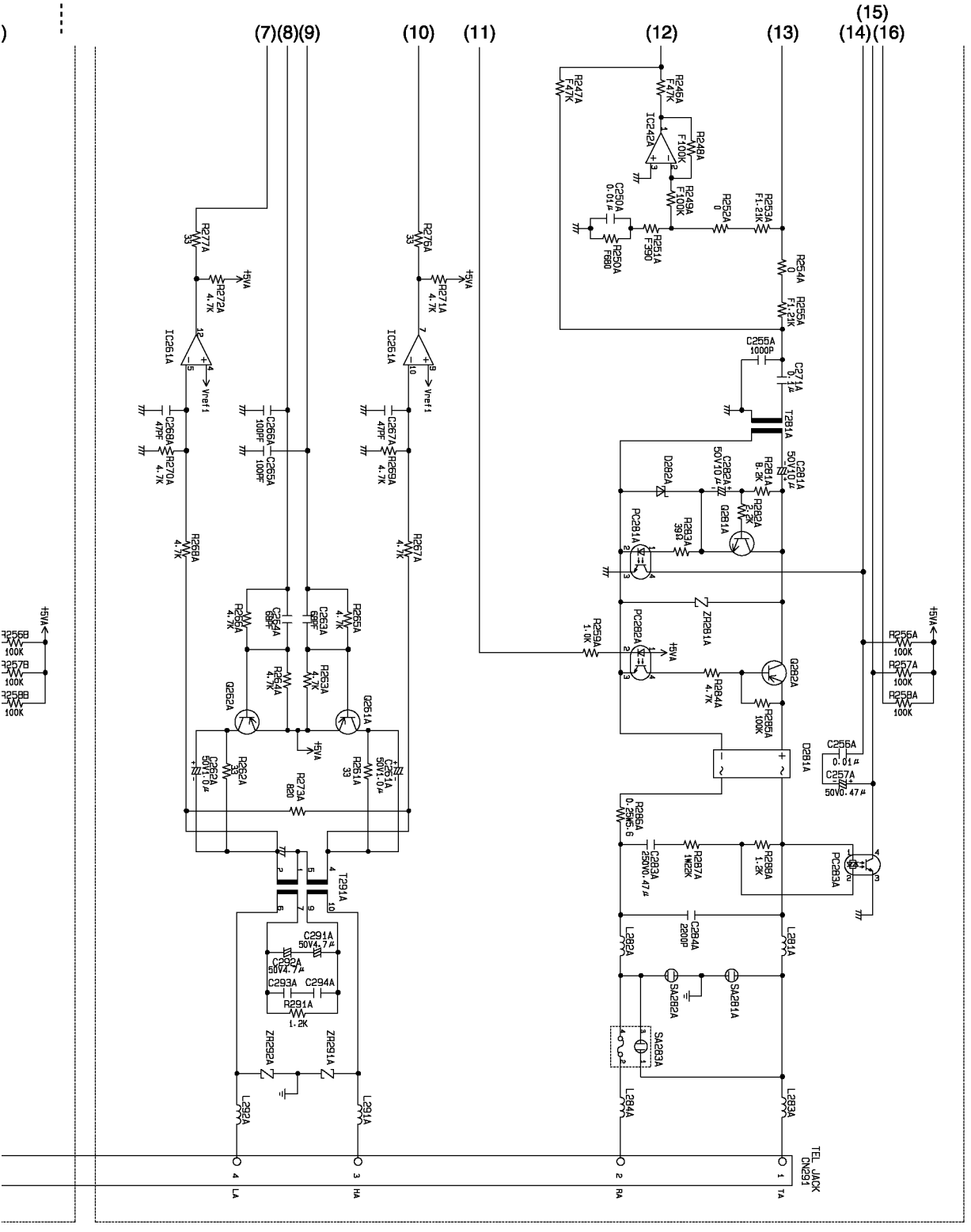



DPITS, APITS I/F CHANNEL-A
KX-TVS102 (CO CARD)(OPTION) No.1
CN201 PIN ASSIGNMENT (SOLDER SIDE VIEW)
DSP I/F 30P CN201
CN201
L201 4.7μH
L202 4.7μH
C201 10V220μ
C202 10V220μ
+5V
-5V
ADOUT-A ADOUT-B BELL-A BELL-B CCK-A CCK-B CDET-A CDET-B DIGL-A DIGL-B DIGS-A DIGS-B DRA-A DRA-B DTA-A DTA-B PULSE-A PULSE-B RVRS-A RVRS-B TSO-X TS1-X
IC241A
IC242A
IC243A
IC244A
IC261A
Vref
(7)(8)(9)
(10)
(11)
(12)
(13)
(14)(16)
(15)


+5VA
R256B 100K
R257B 100K
R258B 100K
C256B 0.01μ
C257B 50V0.47μ
PC283B
(5)
(4)(6)
(3)
(2)
(1)
R254B 0
R255B F1.21K
C271B 0.1μ
T281B
C281B 50V10μ
R253B F1.21K
R252B 0
C255B 1000P
R281B 8.2K
R282B 2.2K
C282B 50V10μ
Q281B
Q282B
D281B
R285B 100K
R284B 4.7K
ZR281B
R283B 39Ω
D282B
PC281B
PC282B
R259B 1.0K
R288B 1.2K
R287B 1W22K
C283B 250V0.47μ
R286B 0.25W5.6
L281B
L283B
L282B
L284B
C284B 2200P
SA281B
SA282B
SA283B
R248B F100K
R245B F47K
R249B F100K
IC242B
R251B F390
C250B 0.01μ
R250B F680
R247B F47K
5 TB
6 RB
N.C. 7 HB
N.C. 8 LB
C233B 20.1μ
IC242B
C235B 20.1μ
IC243B
IC244B
C237B 20.1μ
-5VA
C272B 20.1μ

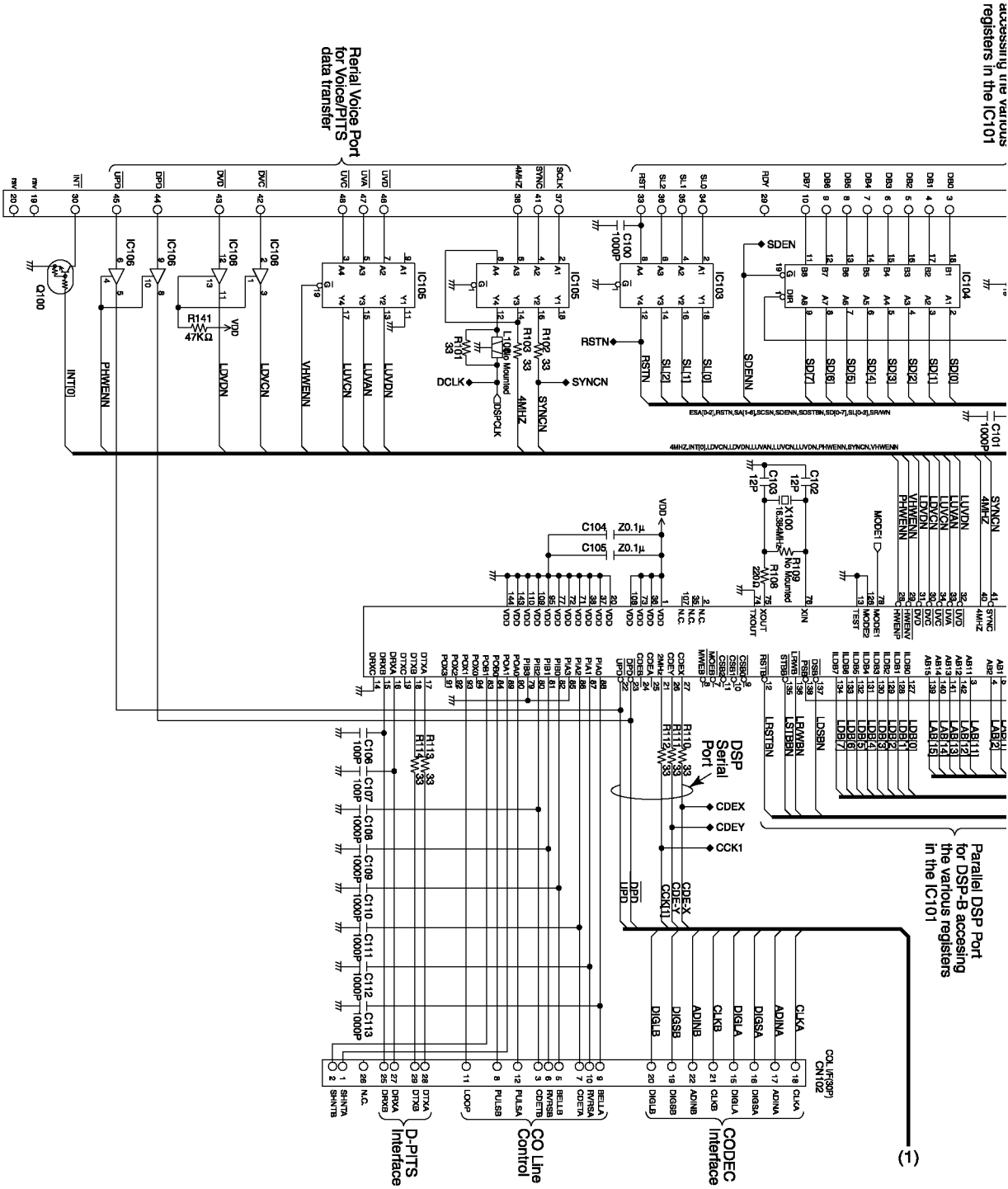

CN291 PIN ASSIGNMENT
(SOLDER SIDE VIEW)
RA LA RB LB
HA TA HB TB

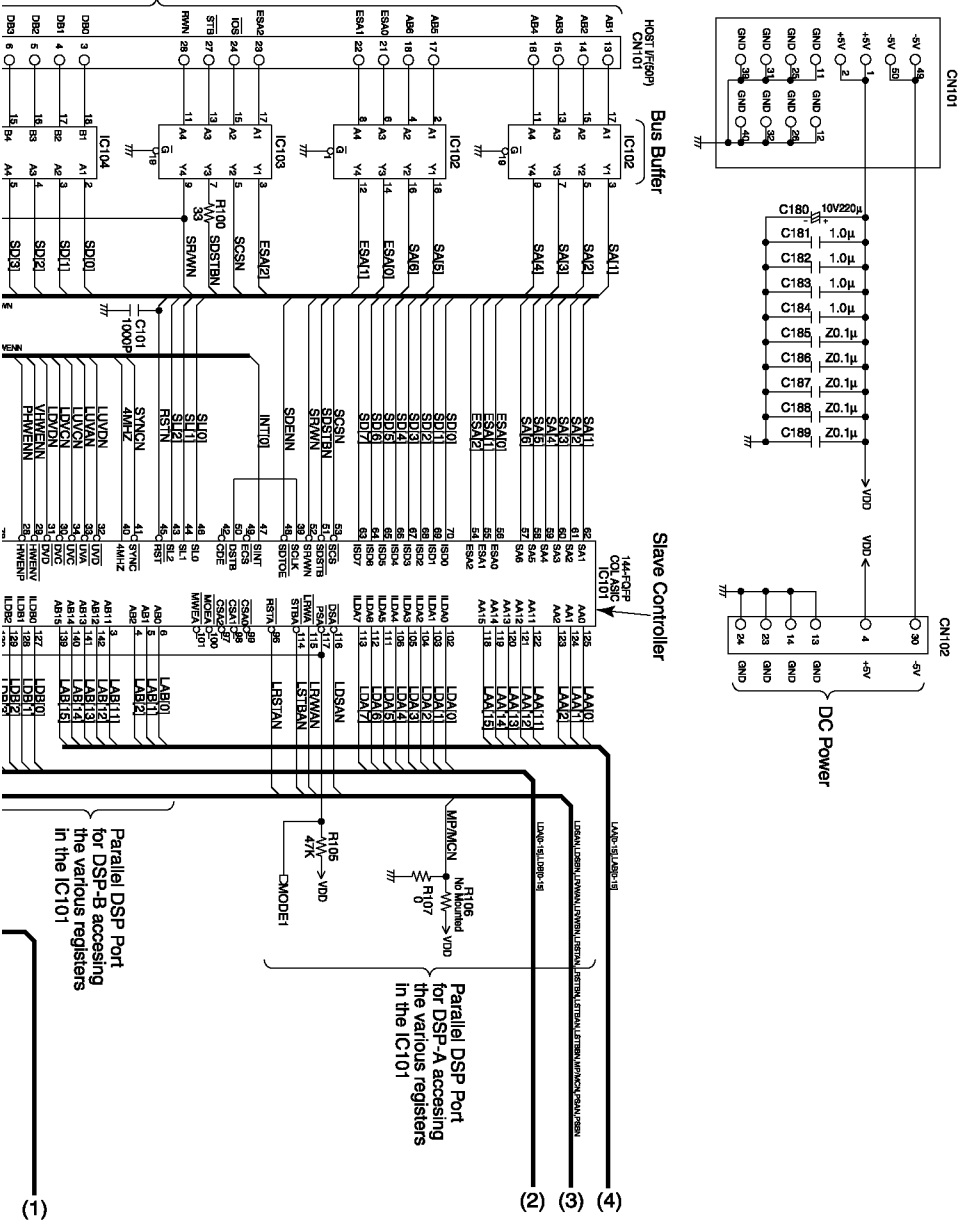

FG_Base
SA280
PQVDDSSV301Y



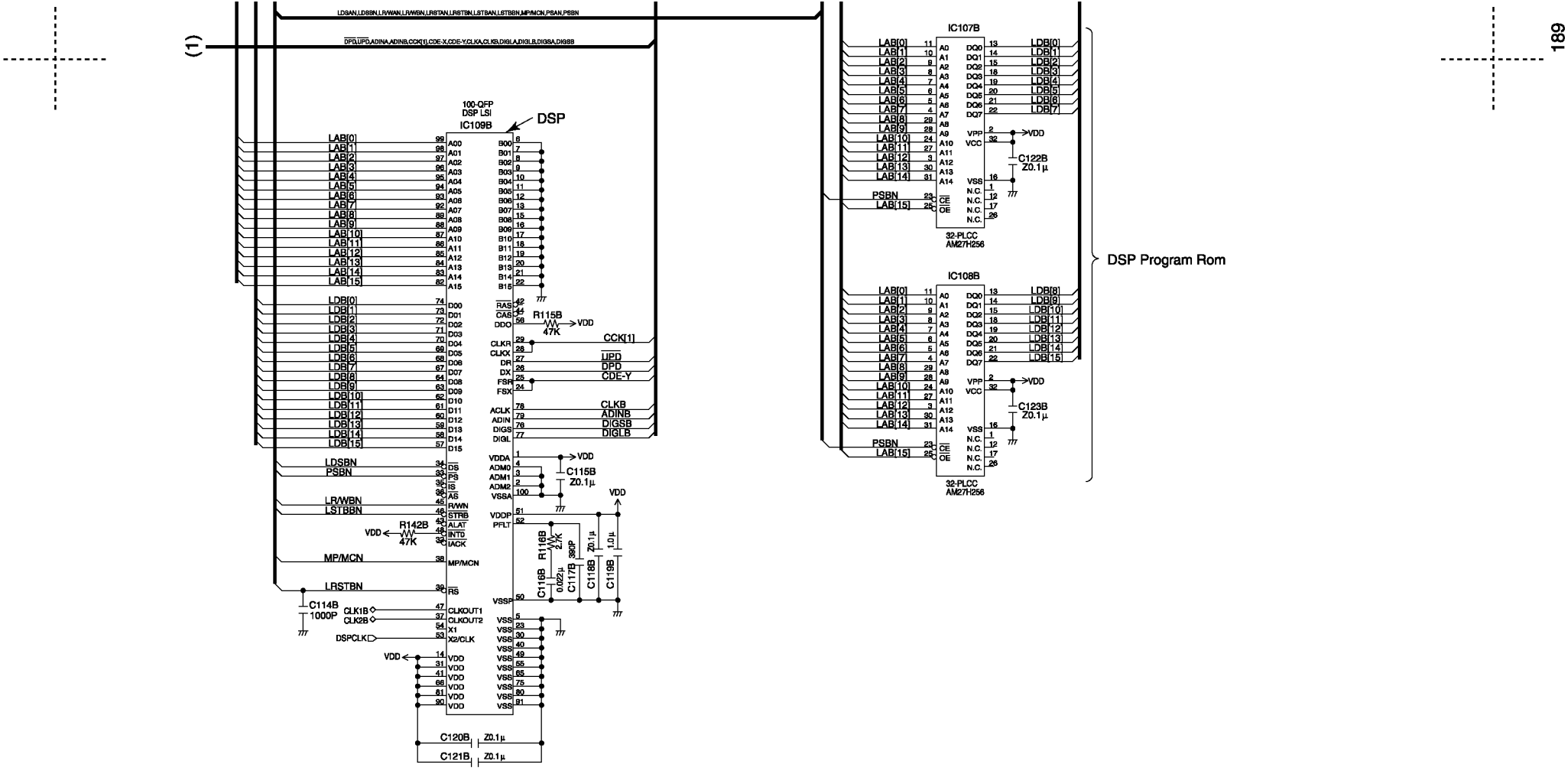
KX-TVS102 (CO CARD)(OPTION) No.2

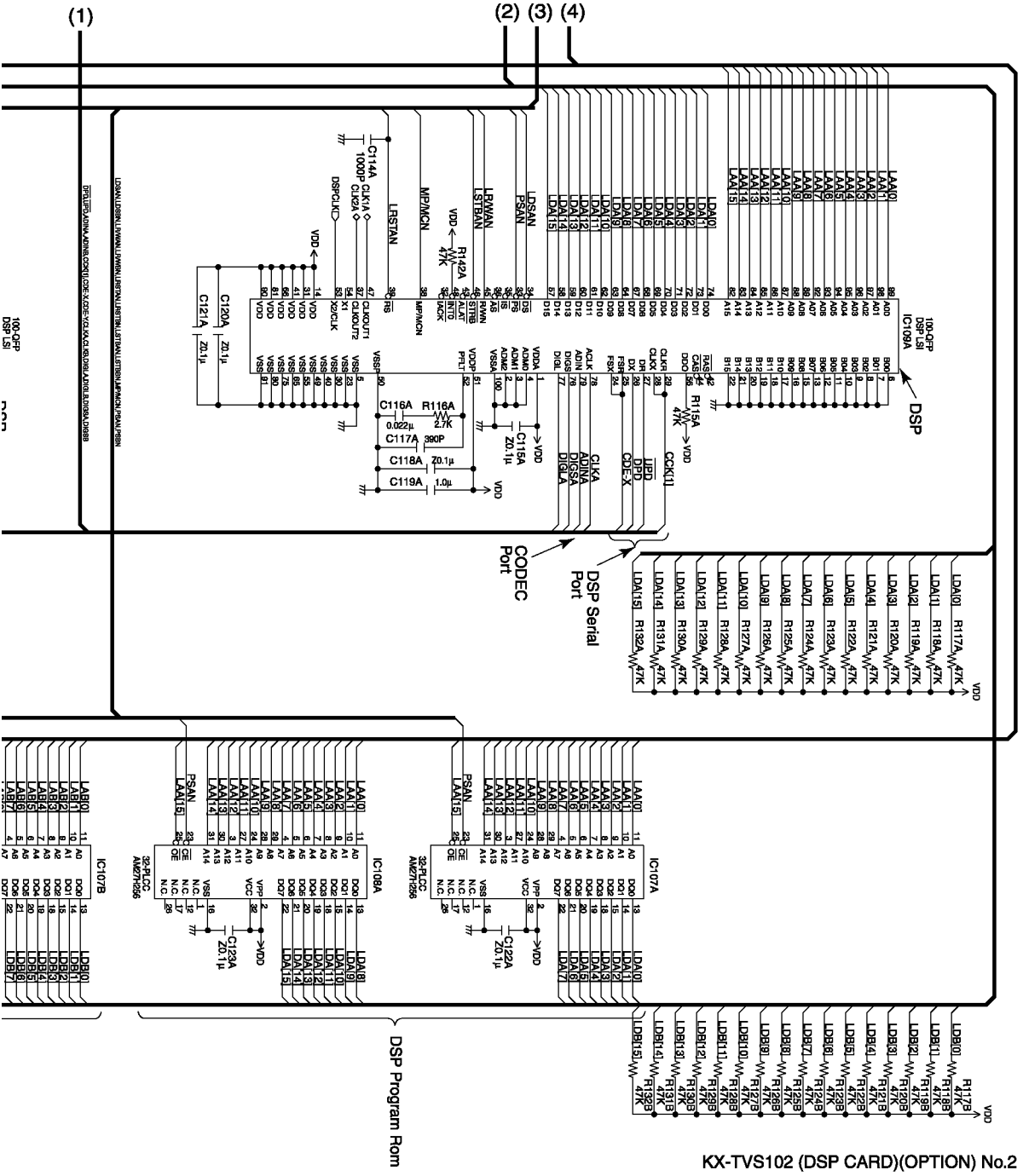
22.5. DPS CARD (KX-TVS102)(OPTION)



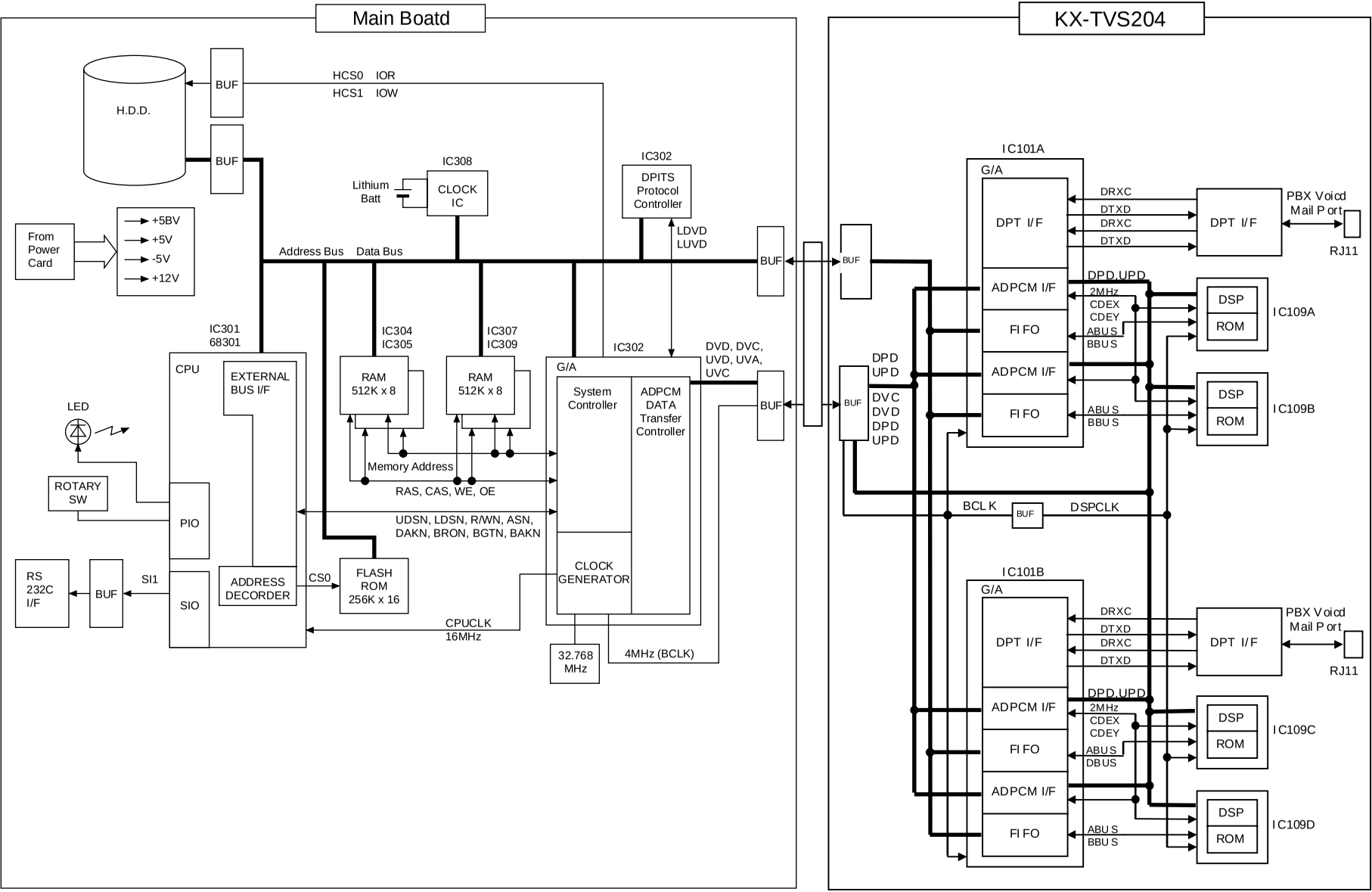

Parallel microprocessor Port for microprocessor accessing the various registers in the IC101
Bus Buffer
Slave Controller
Parallel DSP Port for DSP-B accesing the various registers in the IC101
Parallel DSP Port for DSP-A accesing the various registers in the IC101
DC Power
(1)
(2) (3) (4)

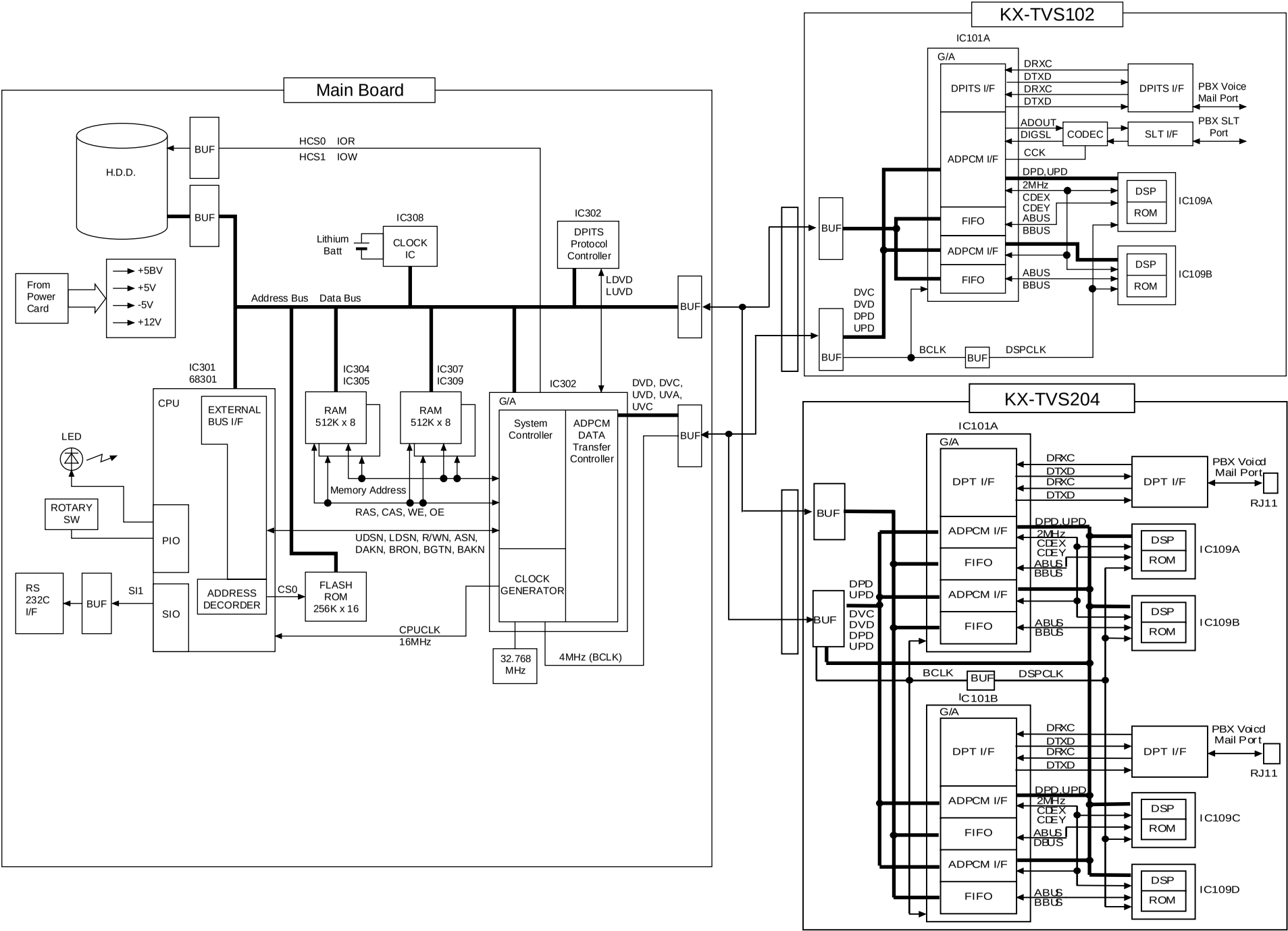
KX-TVS102 (DSP CARD)(OPTION) No.1

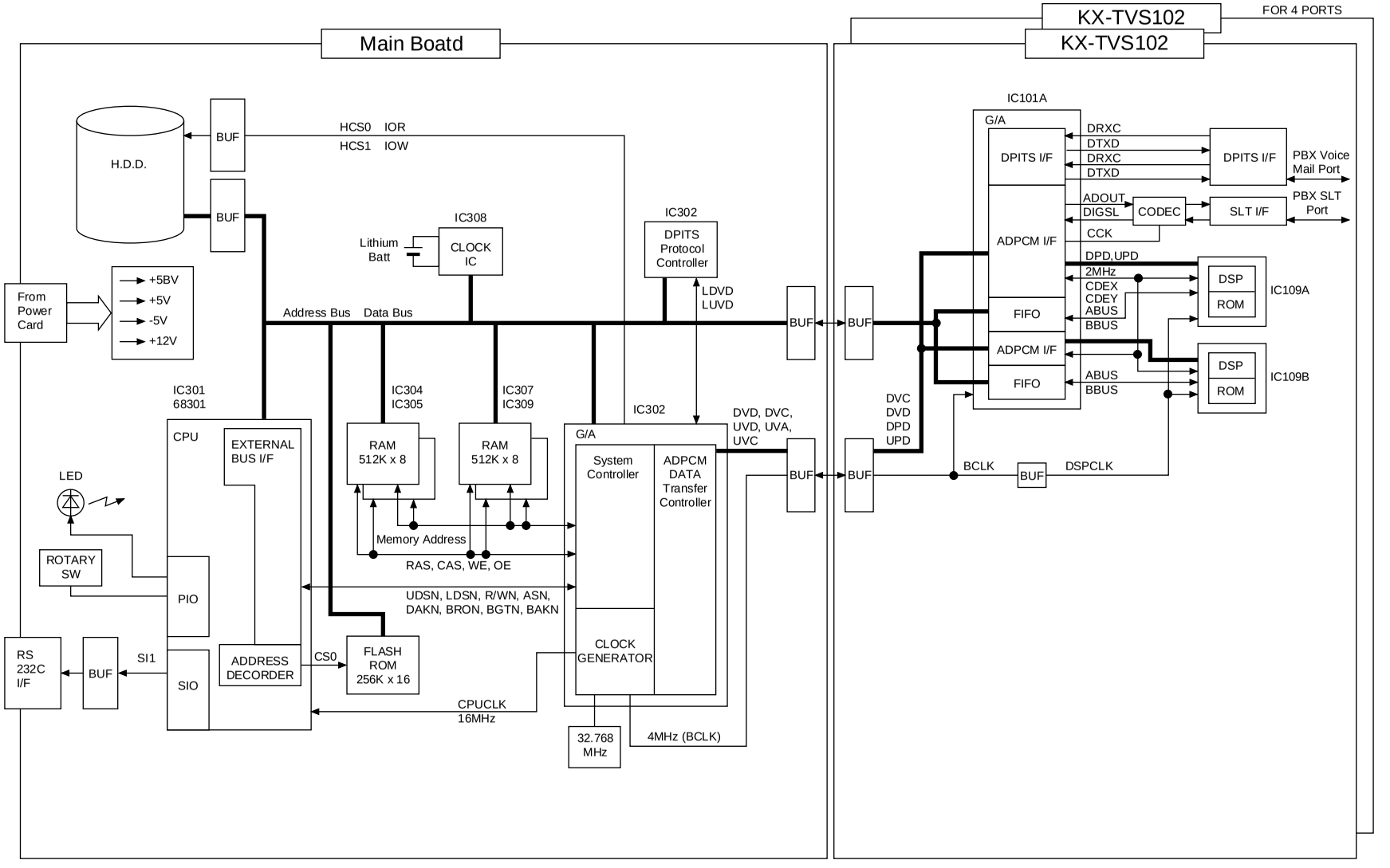

LDSAN,LDSBN,LRWAN,LRWBN,LRSTAN,LRSTBN,LSTAAN,LSTBBN,MP/MCN,PSAN,PSBN
DPD,UPD,ADINA,ADINB,CCK(1),CDE-Y,CLKA,CLKB,DIGLA,DIGLB,DIGSA,DIGSB
(1)
100-QFP
DSP LSI
IC109B
DSP
LAB[0]
LAB[1]
LAB[2]
LAB[3]
LAB[4]
LAB[5]
LAB[6]
LAB[7]
LAB[8]
LAB[9]
LAB[10]
LAB[11]
LAB[12]
LAB[13]
LAB[14]
LAB[15]
LDB[0]
LDB[1]
LDB[2]
LDB[3]
LDB[4]
LDB[5]
LDB[6]
LDB[7]
LDB[8]
LDB[9]
LDB[10]
LDB[11]
LDB[12]
LDB[13]
LDB[14]
LDB[15]
LDSBN
PSBN
LR/WBN
LSTBBN
MP/MCN
LRSTBN
R142B
47K
C114B
1000P
CLK1B
CLK2B
DSPCLK
R115B
47K
CCK[1]
UPD
DPD
CDE-Y
CLKB
ADINB
DIGSB
DIGLB
C115B
Z0.1µ
R116B
2.7K
380P
Z0.1µ
1.0µ
C116B
0.022µ
C117B
C118B
C119B
C120B
Z0.1µ
C121B
Z0.1µ
IC107B
IC108B
32-PLCC
AM27H256
C122B
Z0.1µ
C123B
Z0.1µ
DSP Program Rom



KX-TVS102 (DSP CARD)(OPTION) No.2

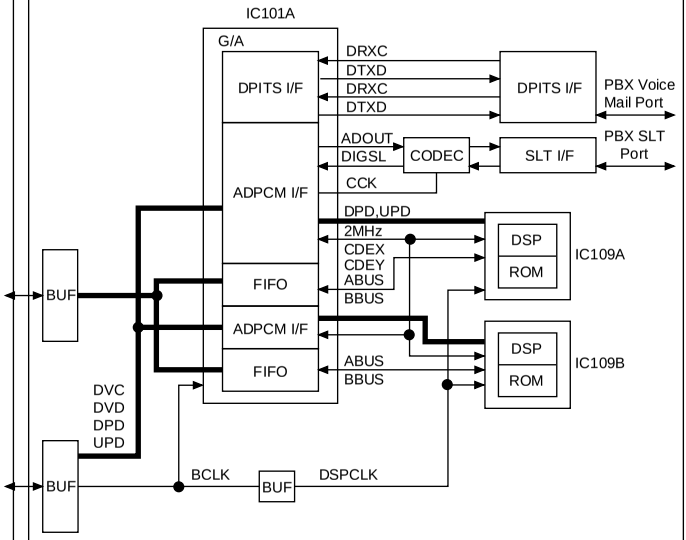

Main Boatd
KX-TVS204
H.D.D.
BUF
BUF
HCS0 IOR
HCS1 IOW
IC308
Lithium Batt
CLOCK IC
IC302
DPITS Protocol Controller
LDVD
LUVD
From Power Card
+5BV
+5V
-5V
+12V
Address Bus
Data Bus
BUF
IC301
68301
CPU
EXTERNAL BUS I/F
IC304
IC305
IC307
IC309
RAM 512K x 8
RAM 512K x 8
IC302
G/A
System Controller
ADPCM DATA Transfer Controller
DVD, DVC, UVD, UVA, UVC
BUF
LED
ROTARY SW
PIO
Memory Address
RAS, CAS, WE, OE
UDSN, LDSN, R/WN, ASN, DAKN, BRON, BGTN, BAKN
CLOCK GENERATOR
RS 232C I/F
BUF
SI1
SIO
ADDRESS DECORDER
CS0
FLASH ROM 256K x 16
CPUCLK 16MHz
32.768 MHz
4MHz (BCLK)
BUF
BUF
DPD
UPD
DVC
DVD
DPD
UPD
IC101A
G/A
DPT I/F
DRXC
DTXD
DRXC
DTXD
DPT I/F
PBX Voicd Mail Port
RJ11
ADPCM I/F
FIFO
ADPCM I/F
FIFO
DPD,UPD
2MHz
CDEX
CDEY
ABUS
BBUS
ABUS
BBUS
DSP
ROM
IC109A
DSP
ROM
IC109B
BCLK
BUF
DSPCLK
IC101B
G/A
DPT I/F
DRXC
DTXD
DRXC
DTXD
DPT I/F
PBX Voicd Mail Port
RJ11
ADPCM I/F
FIFO
ADPCM I/F
FIFO
DPD,UPD
2MHz
CDEX
CDEY
ABUS
DBUS
ABUS
BBUS
DSP
ROM
IC109C
DSP
ROM
IC109D


Main Board
H.D.D.
BUF
BUF
HCS0 IOR
HCS1 IOW
IC308
Lithium Batt
CLOCK IC
IC302
DPITS Protocol Controller
From Power Card
+5BV
+5V
-5V
+12V
Address Bus Data Bus
LDVD
LUVD
BUF
IC301
68301
CPU
EXTERNAL BUS I/F
IC304
IC305
RAM 512K x 8
IC307
IC309
RAM 512K x 8
IC302
G/A
System Controller
ADPCM DATA Transfer Controller
DVD, DVC, UVD, UVA, UVC
BUF
LED
ROTARY SW
PIO
Memory Address
RAS, CAS, WE, OE
UDSN, LDSN, R/WN, ASN, DAKN, BRON, BGTN, BAKN
RS 232C I/F
BUF
SI1
SIO
ADDRESS DECORDER
CS0
FLASH ROM 256K x 16
CLOCK GENERATOR
CPUCLK 16MHz
32.768 MHz
4MHz (BCLK)
KX-TVS102
IC101A
G/A
DPITS I/F
DRXC
DTXD
DRXC
DTXD
DPITS I/F
PBX Voice Mail Port
ADPCM I/F
ADOUT
DIGSL
CODEC
SLT I/F
PBX SLT Port
CCK
DPD,UPD
2MHz
CDEX
CDEY
ABUS
BBUS
FIFO
DSP
ROM
IC109A
ADPCM I/F
FIFO
DSP
ROM
IC109B
BUF
DVC
DVD
DPD
UPD
BUF
BCLK
BUF
DSPCLK
KX-TVS204
IC101A
G/A
DPT I/F
DRXC
DTXD
DRXC
DTXD
DPT I/F
PBX Voicd Mail Port
RJ11
ADPCM I/F
DPD,UPD
2MHz
CDEX
CDEY
ABUS
BBUS
FIFO
DSP
ROM
IC109A
ADPCM I/F
FIFO
DSP
ROM
IC109B
BUF
DPD
UPD
DVC
DVD
DPD
UPD
BUF
BCLK
BUF
DSPCLK
IC101B
G/A
DPT I/F
DRXC
DTXD
DRXC
DTXD
DPT I/F
PBX Voicd Mail Port
RJ11
ADPCM I/F
DPD,UPD
2MHz
CDEX
CDEY
ABUS
DBUS
FIFO
DSP
ROM
IC109C
ADPCM I/F
FIFO
DSP
ROM
IC109D

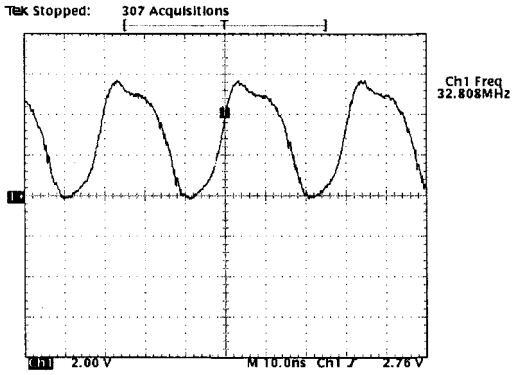

Main Boatd
KX-TVS102
KX-TVS102
FOR 4 PORTS
H.D.D.
BUF
BUF
HCS0 IOR
HCS1 IOW
IC308
Lithium Batt
CLOCK IC
IC302
DPITS Protocol Controller
From Power Card
+5BV
+5V
-5V
+12V
Address Bus
Data Bus
LDVD
LUVD
BUF
BUF
IC101A
G/A
DPITS I/F
DRXC
DTXD
DRXC
DTXD
DPITS I/F
PBX Voice Mail Port
ADOUT
DIGSL
CODEC
SLT I/F
PBX SLT Port
ADPCM I/F
CCK
DPD,UPD
2MHz
CDEX
CDEY
ABUS
BBUS
FIFO
DSP
ROM
IC109A
ADPCM I/F
FIFO
DSP
ROM
IC109B
ABUS
BBUS
IC301
68301
CPU
EXTERNAL BUS I/F
IC304
IC305
RAM 512K x 8
IC307
IC309
RAM 512K x 8
IC302
G/A
System Controller
ADPCM DATA Transfer Controller
DVD, DVC, UVD, UVA, UVC
DVC
DVD
DPD
UPD
BUF
BUF
BCLK
BUF
DSPCLK
LED
ROTARY SW
PIO
Memory Address
RAS, CAS, WE, OE
UDSN, LDSN, R/WN, ASN, DAKN, BRON, BGTN, BAKN
RS 232C I/F
BUF
SI1
SIO
ADDRESS DECORDER
CS0
FLASH ROM 256K x 16
CLOCK GENERATOR
CPUCLK 16MHz
32.768 MHz
4MHz (BCLK)

KX-TVS102

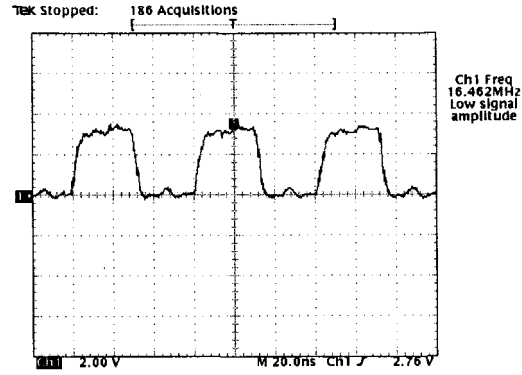
KX-TVS120



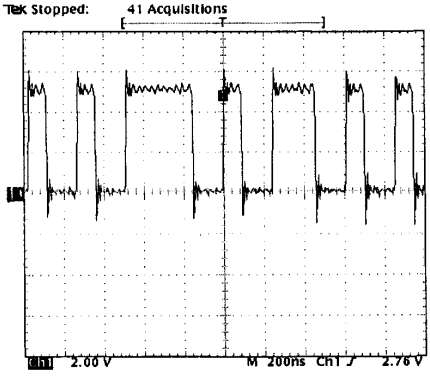
① XOUT



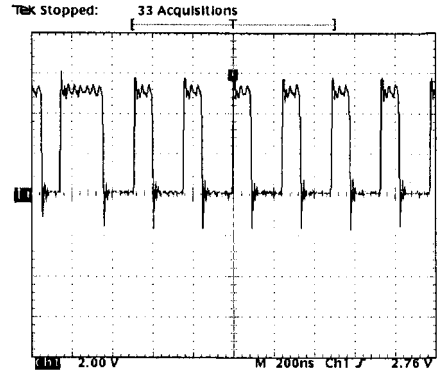
② CPU CLK



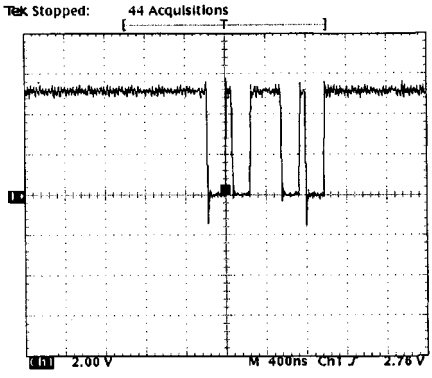
③ UDSN



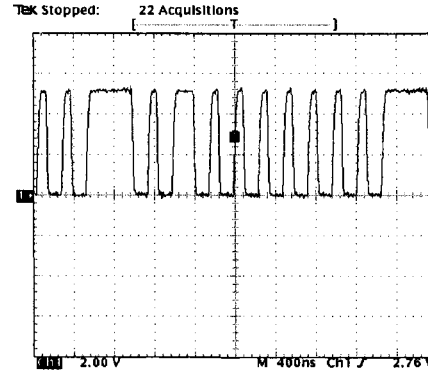
④ LDSN



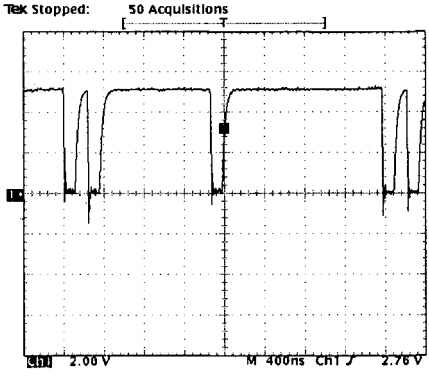
⑤ R/WN



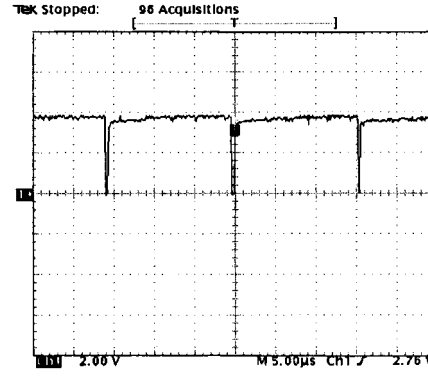
⑥ ASN



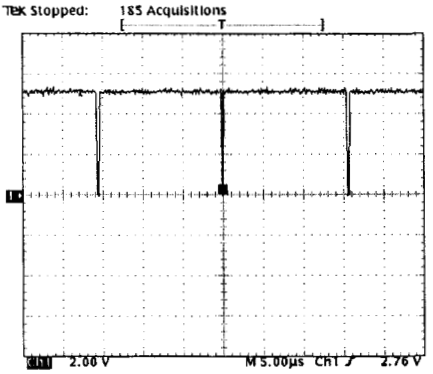
⑦ DAKN



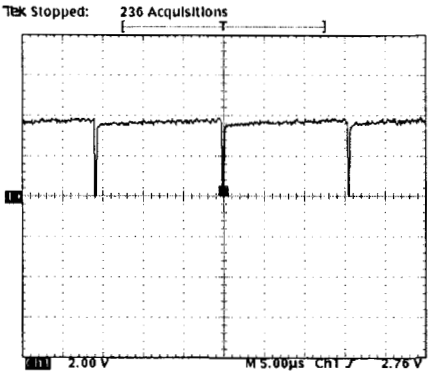
⑧ BRON



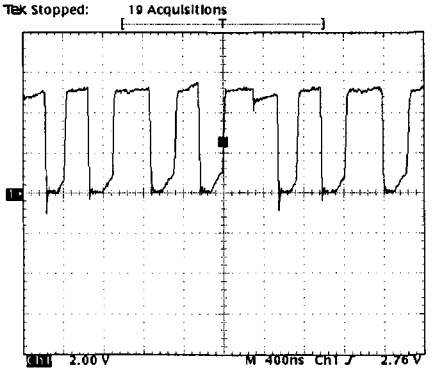
⑨ BGTN



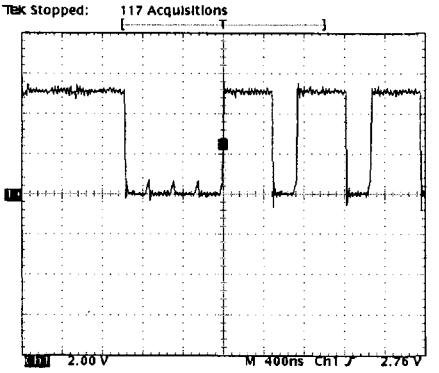
⑩ BAKN



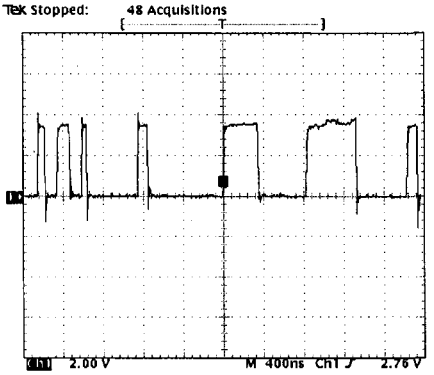
⑪ D0~D15



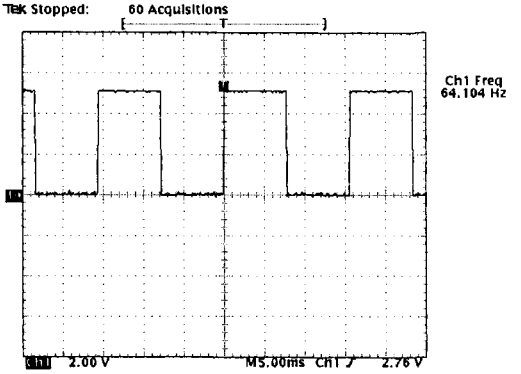
⑫ A0~A23



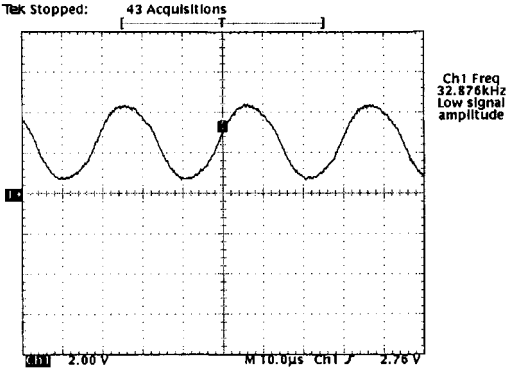
⑬ MA0~MA9



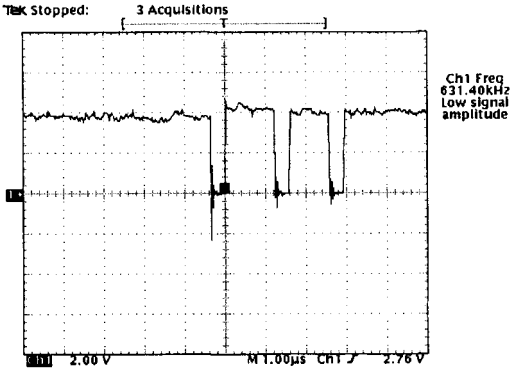
⑭ STDP



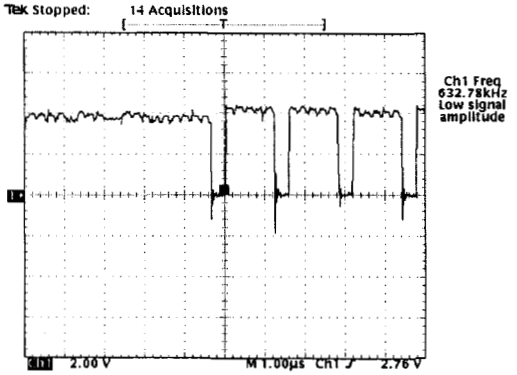
⑮ XT



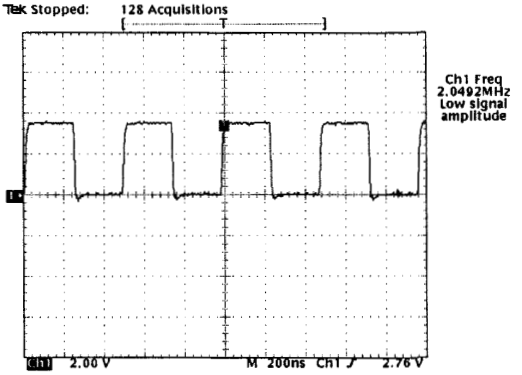
⑯ RTCSN



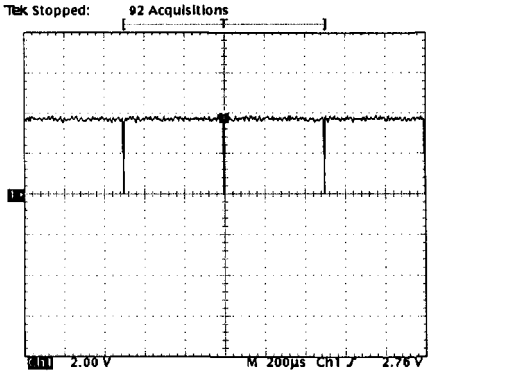
⑰ HDLCSN



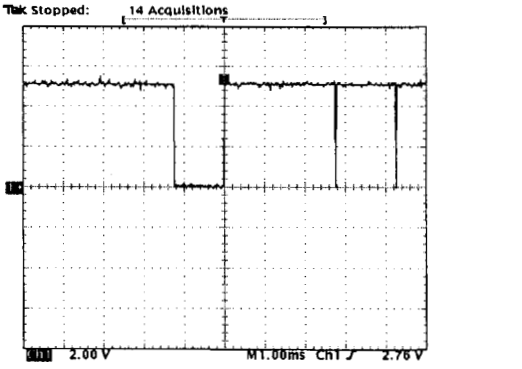
⑱ 2MHz



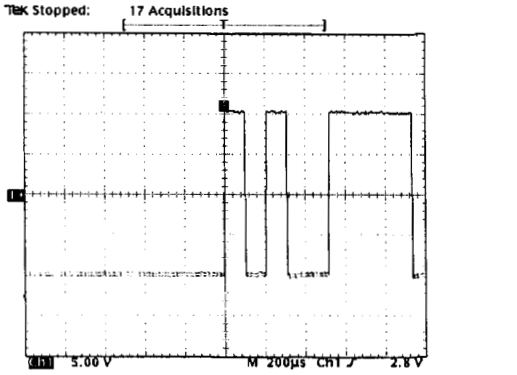
⑲ CENIN



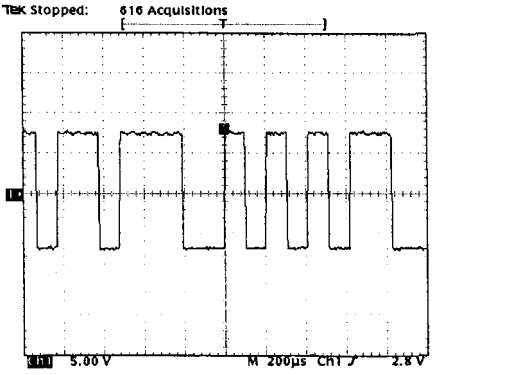
⑳ DPINTN



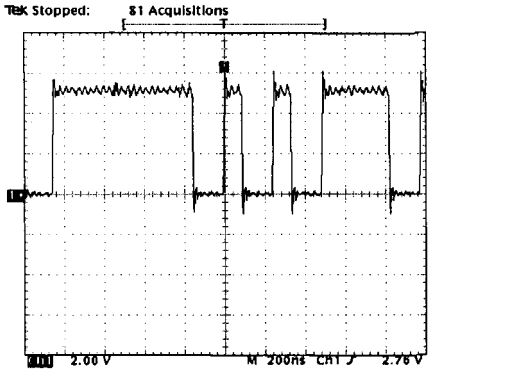
㉑ RXD



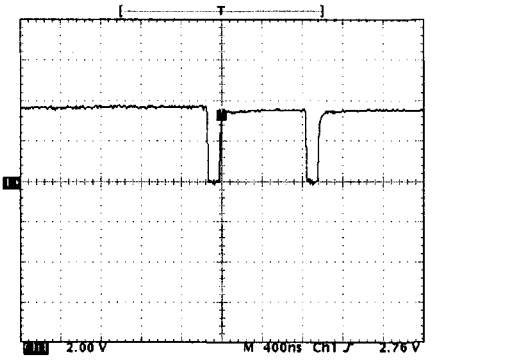
㉒ TXD



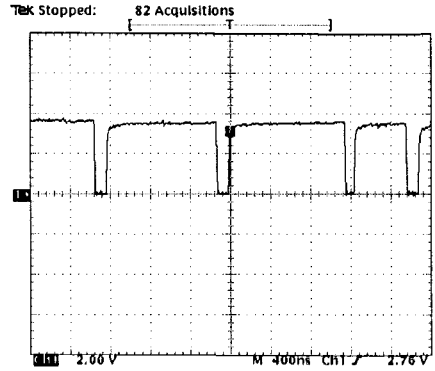
㉓ ROMCSN



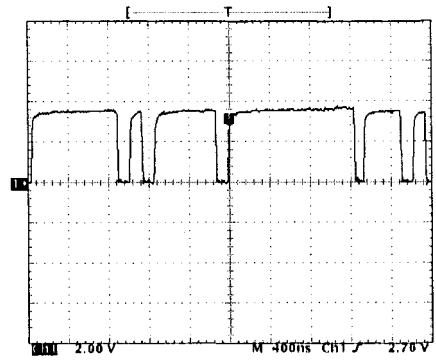
㉔ RASON



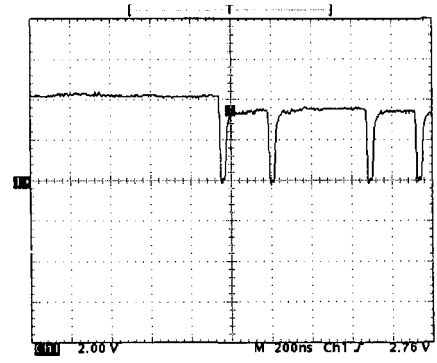
㉕ RASIN



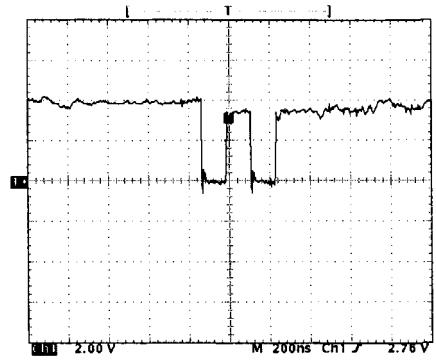
㉖ CASN



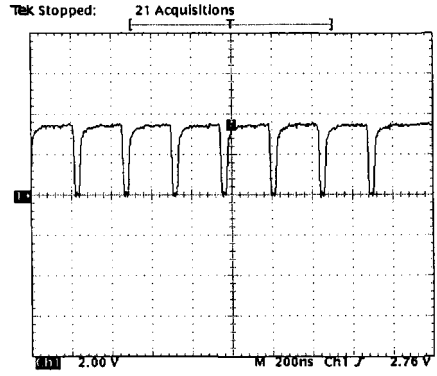
㉗ UWEN



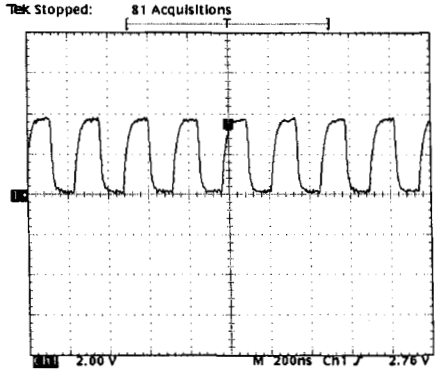
㉘ MOEN



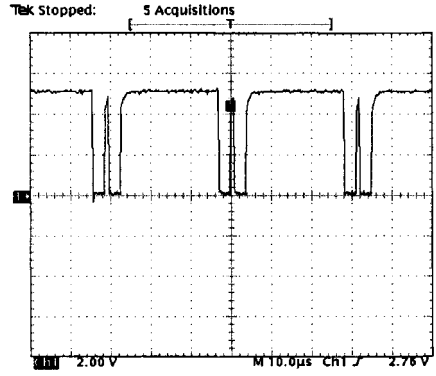
㉙ LWEN



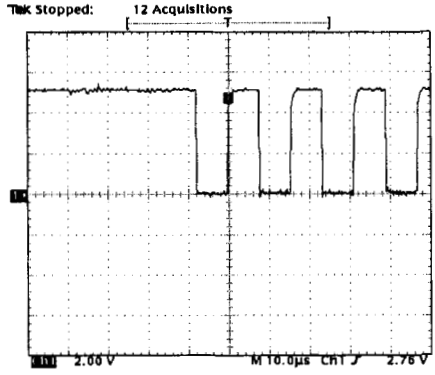
㉚ BCLK



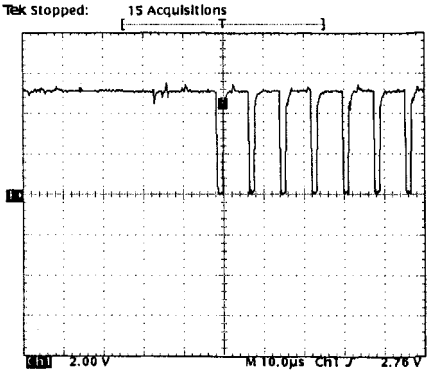
㉛ UPDN



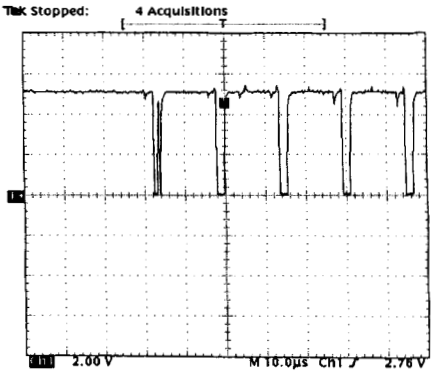
㉜ UVDN



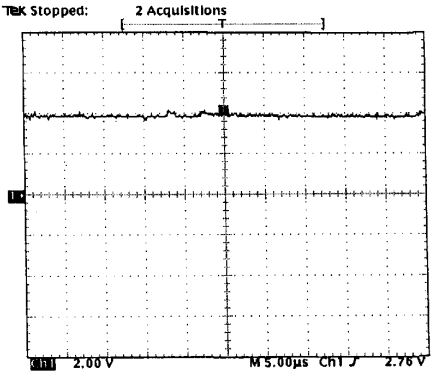
㉝ UVAN



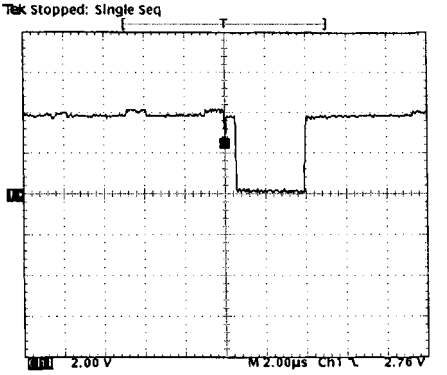
㉞ UVCN



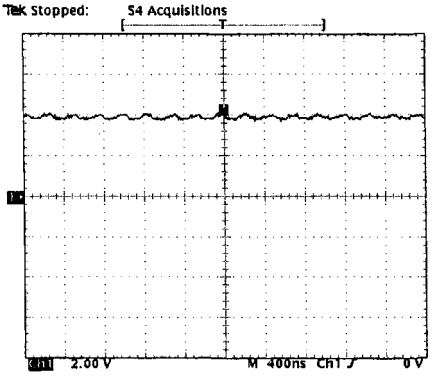
㉟ DPDN



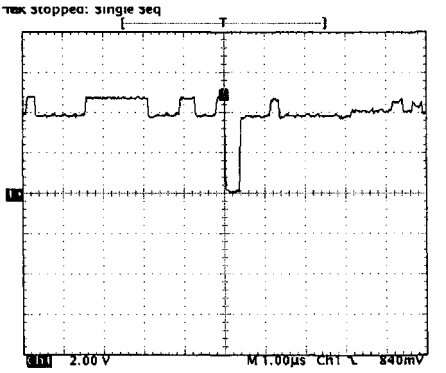
㊱ DVDN



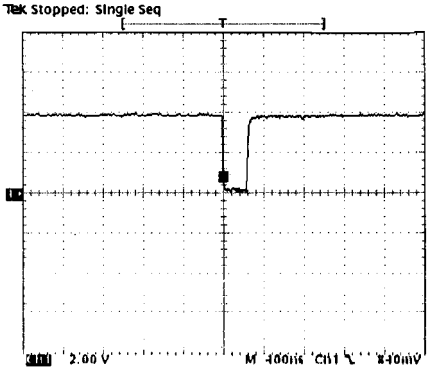
㊲ DVCN



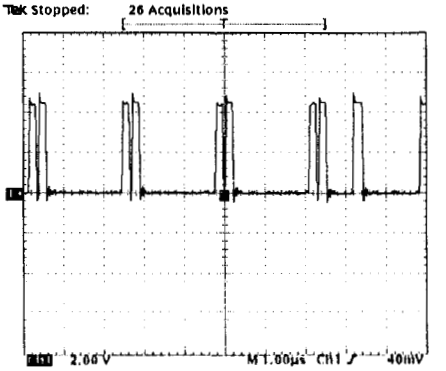
㊳ IOSON



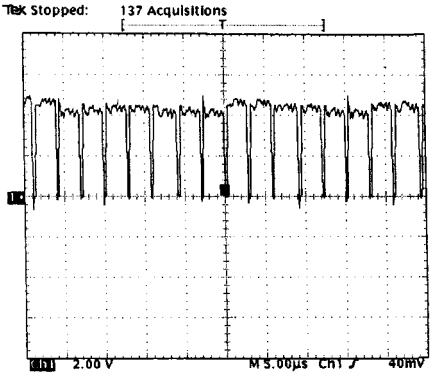
㊴ SYNCN



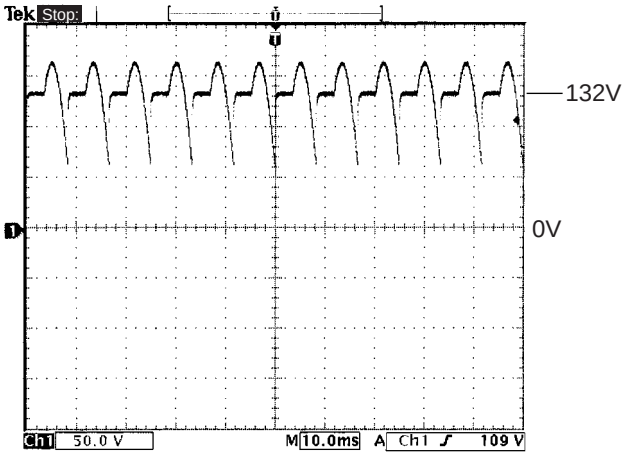
㊵ LDDIR



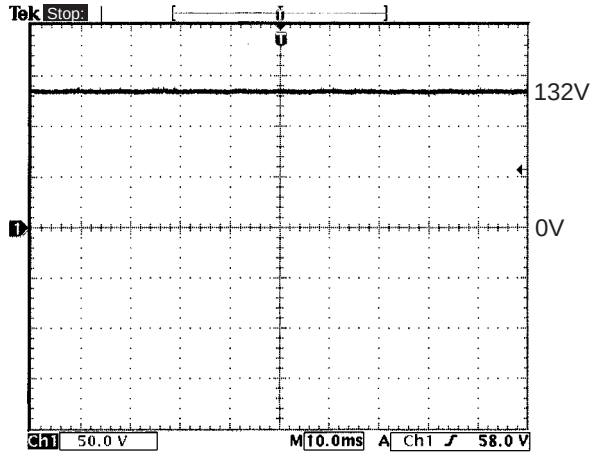
㊶ HDENN



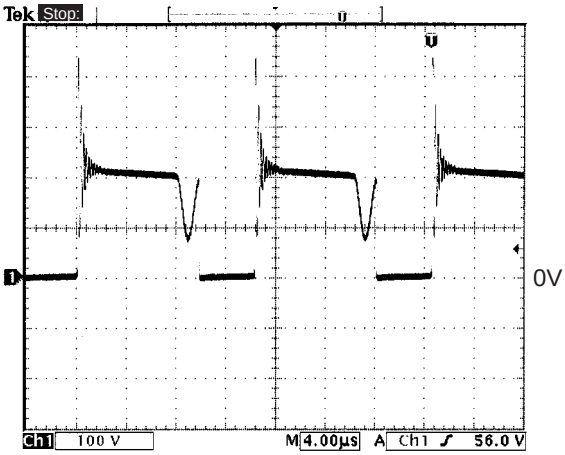
① After diode blidge



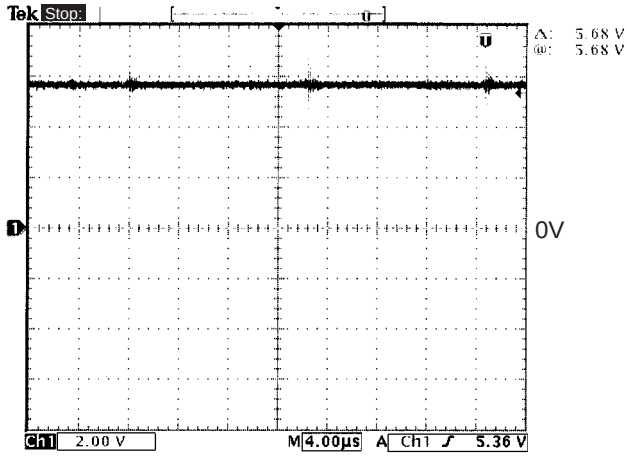
② After rectification



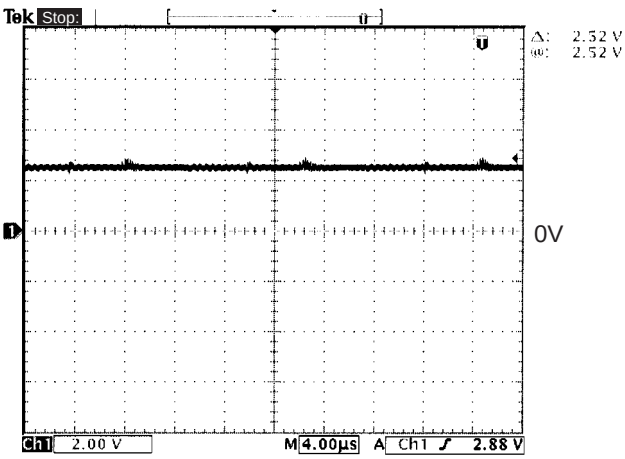
③ FET (D-S)



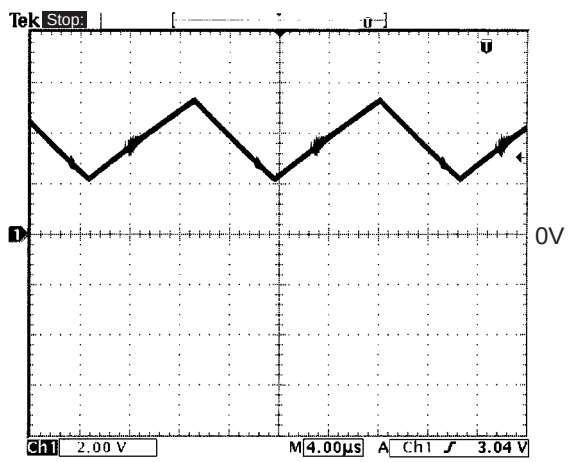
④ IC1-SS



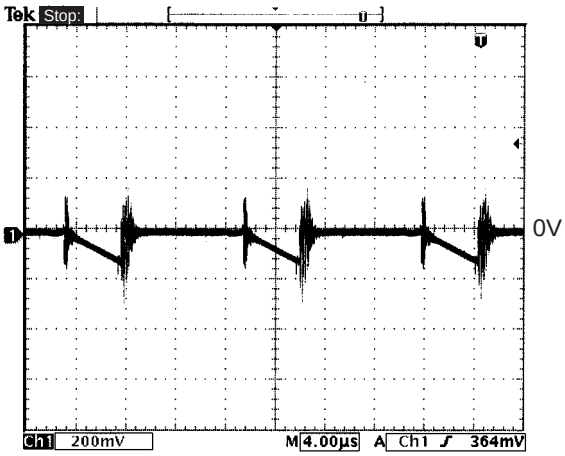
⑤ IC1-RT



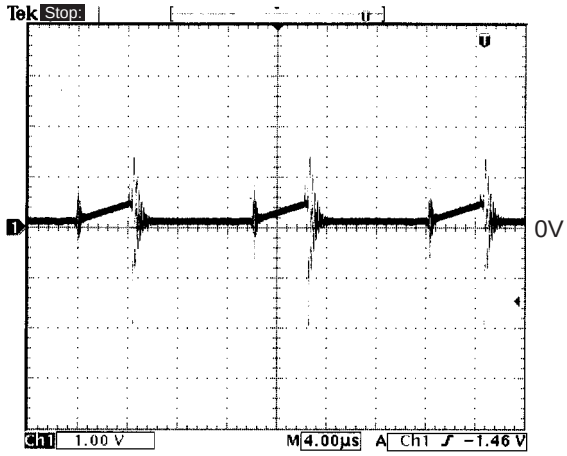
⑥ IC1-CT



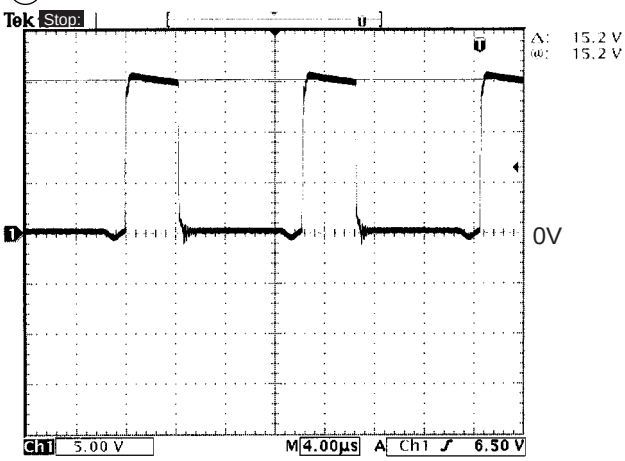
⑦IC1-CLM



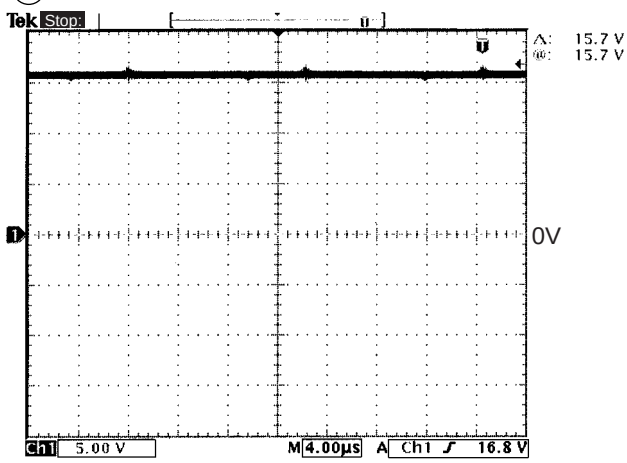
⑧R11



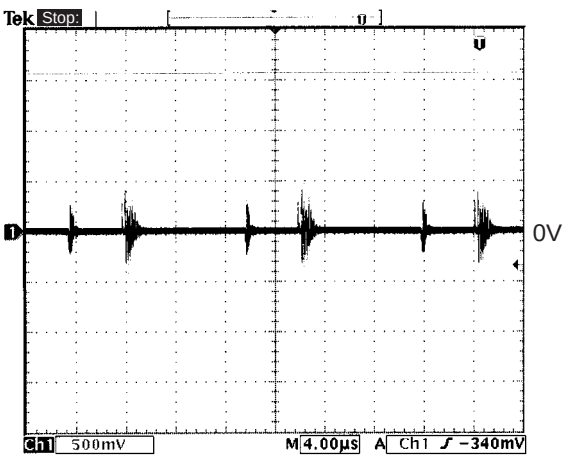
⑨IC1-Vo



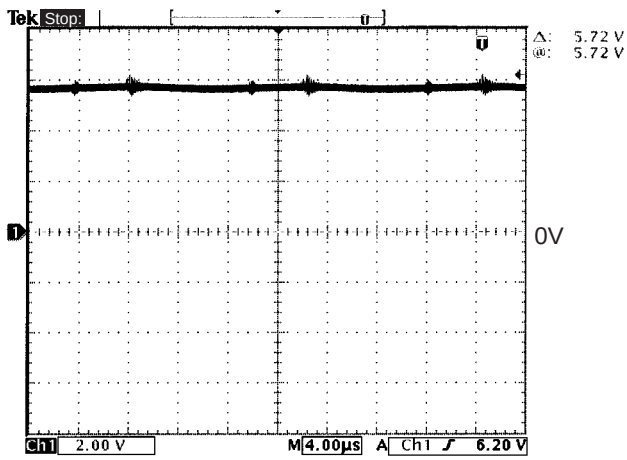
⑩IC1-Vcc



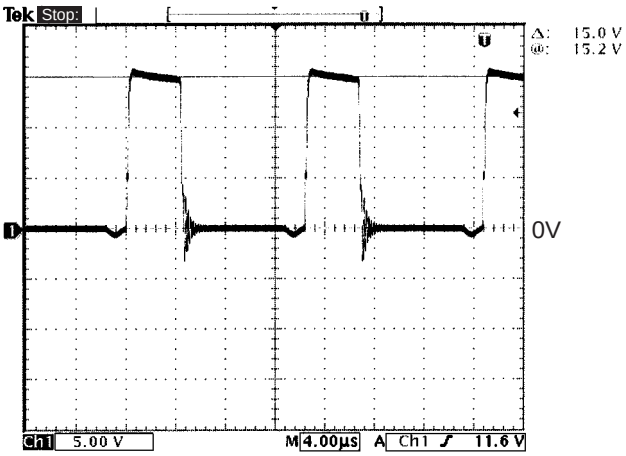
⑪IC1-OVP



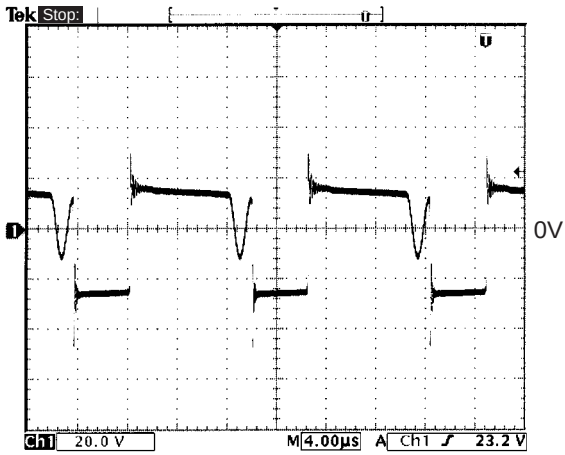
⑫IC1-IFB



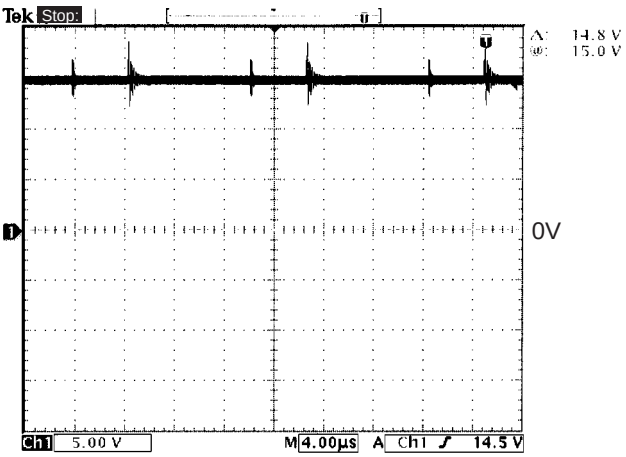
⑬ FET-Gate



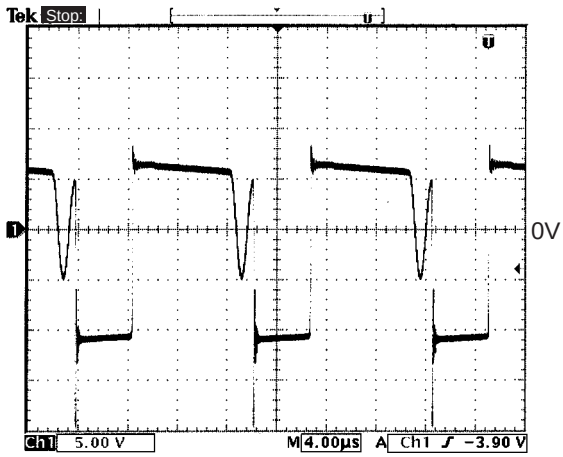
⑭



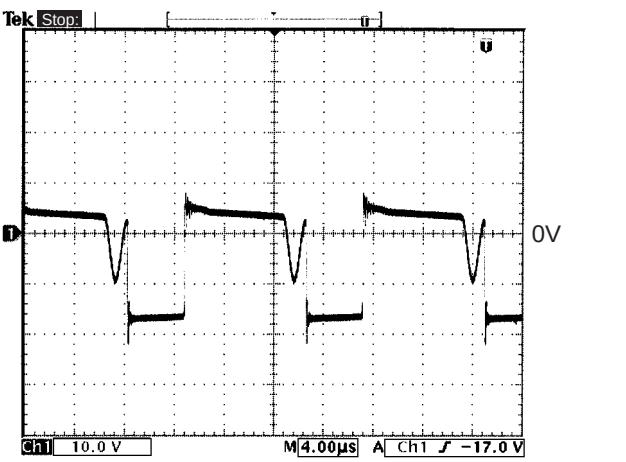
⑮



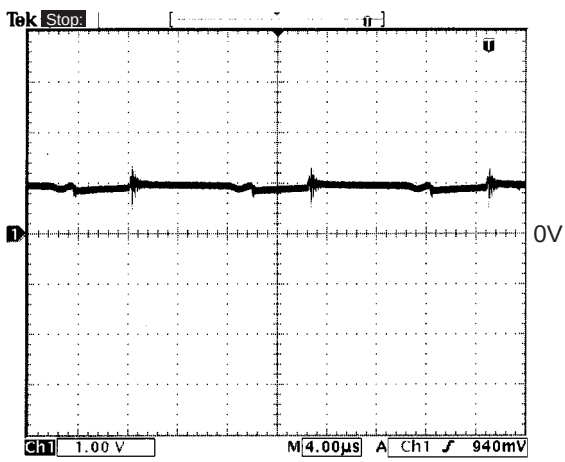
⑯



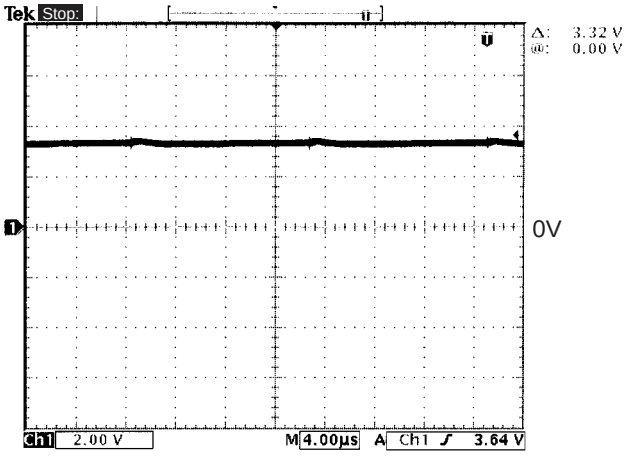
⑰



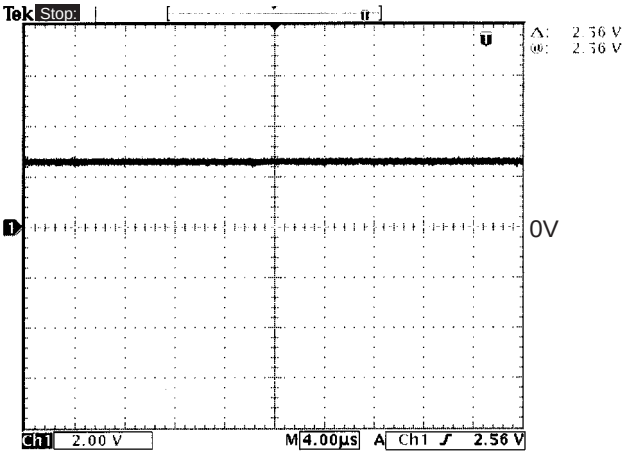
⑱



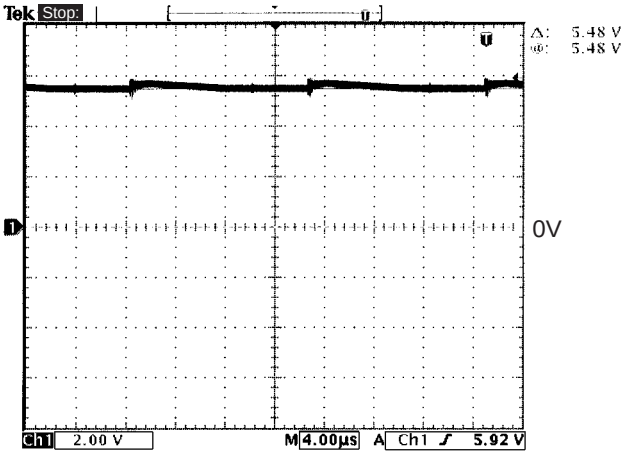
⑲


Tek Stop:
Δ: 3.32 V
@: 0.00 V
0V
Ch1 2.00 V
M 4.00µs A Ch1 3.64 V

⑳

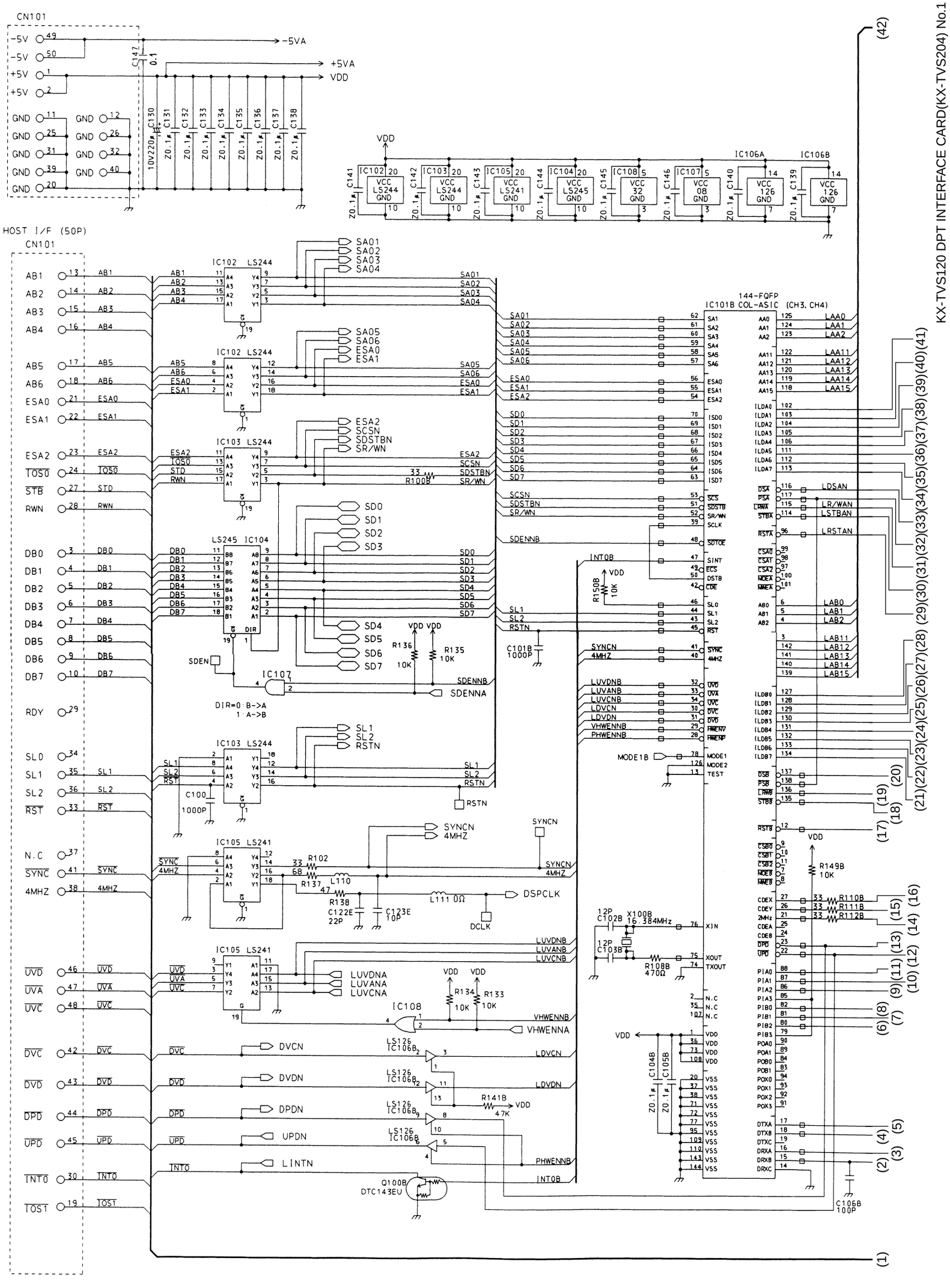

Tek Stop:
Δ: 2.56 V
@: 2.56 V
0V
Ch1 2.00 V
M 4.00µs A Ch1 2.56 V

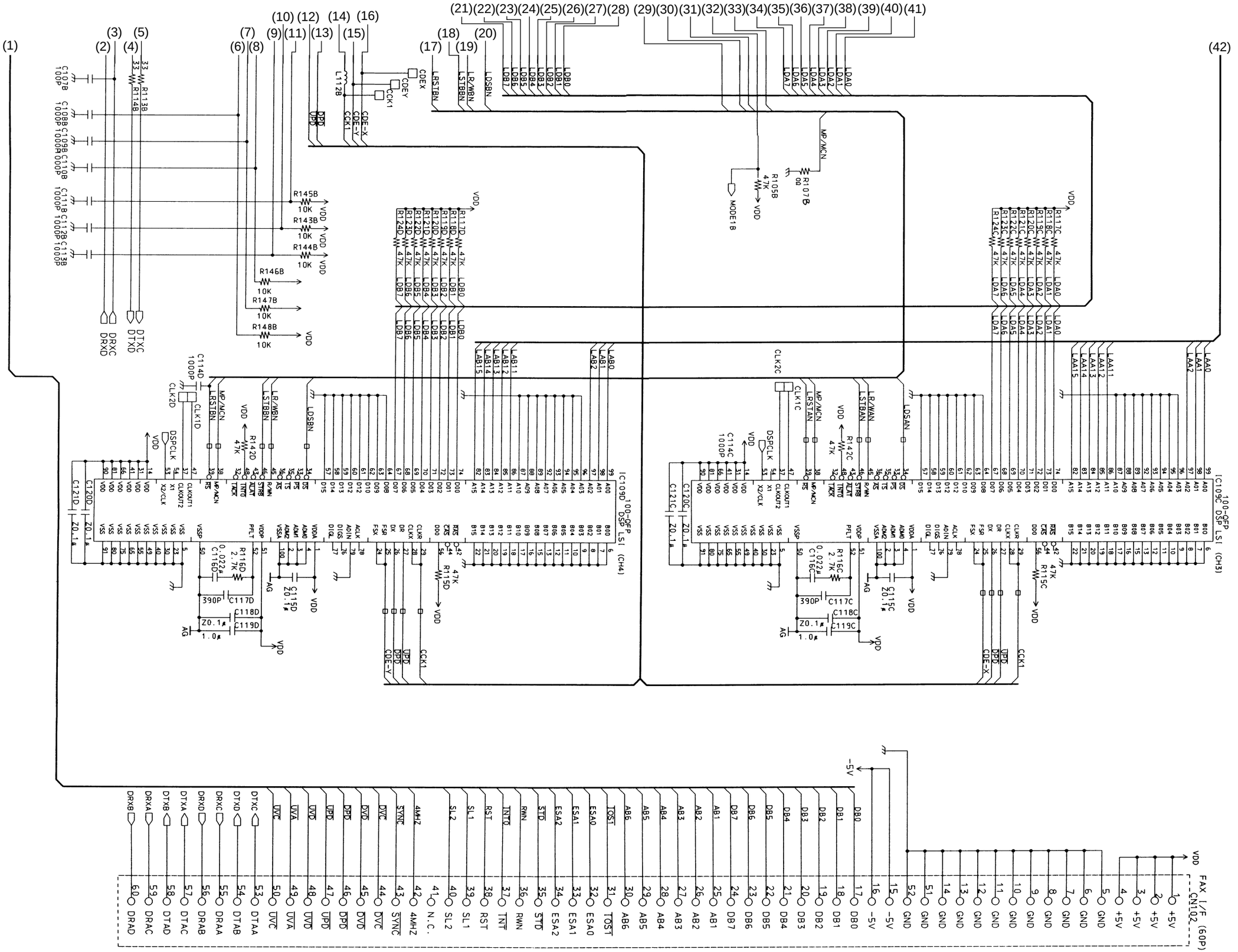
㉑


Tek Stop:
Δ: 5.48 V
@: 5.48 V
0V
Ch1 2.00 V
M 4.00µs A Ch1 5.92 V

POWER SUPPLY CONNECTOR
POWER 12PIN
CN305
DCALM
+12V
H12GND
GND
+5V
-5V
+5VA
H5GND
H5V
J1
Power Circuit
C304 25V100µ
C373 16V330µ
C372 16V330µ
C371 25V100µ
C370 25V100µ
C374 25V100µ
C396 1.0µ
C395 1.0µ
C394 1.0µ
C393 1.0µ
C392 1.0µ
C391 1.0µ
C390 1.0µ
C387 Z0.1µ
C386 Z0.1µ
C385 Z0.1µ
C3C1 Z0.1µ
C3C2 Z0.1µ
C3C3 Z0.1µ
C3C4 Z0.1µ
C3C5 Z0.1µ
C3C6 Z0.1µ
C3C7 Z0.1µ
C3C8 Z0.1µ
C3D4 Z0.1µ
C3D5 Z0.1µ
C3D6 Z0.1µ
C3D7 Z0.1µ
C3D8 Z0.1µ
C3D9 Z0.1µ
C3E0 Z0.1µ
C3E1 Z0.1µ
C3E2 Z0.1µ
C3C9 Z0.1µ
C3D0 Z0.1µ
C3D1 Z0.1µ
C3D2 Z0.1µ
C3D3 Z0.1µ
RS-232C CONNECTOR
CN307
FG
GND
TXD
RXD
DTR
DSR
FGTP
FIL306
FIL305
R3U9 0
0V – +7V – -7V
RS-232C DRIVER
IC311
16-SOP
C326 25V4.7µ
C327 25V4.7µ
C328 25V4.7µ
C325 25V4.7µ
C324 25V100µ
C3E3 Z0.1µ
R3W9 0
R3U0 33
0V
+7V
DIP SW
SW301
DRS3010
R339 47K
R338 47K
R337 47K
R336 47K
POWER LED CONNECTOR
CN306
LEDP
LEDN
R330 220
R3W1 33
+5VA
Q301
R342 10K
0V : EXTERNAL TERMINAL NON : +5V
+10V : TERMINAL CONNECT : 0V
EXTERNAL
LED BOARD
TM801
D801
R801 220
PSUP1139XA-B
POWER ON : 5.0V
POWER OFF : MORE THAN2.8V
LITHIUM BATTERY FOR TIME DATA BACK UP
BAT301
JMP1
D301
MRSTN
D300
VBB
R376 10K
STDP
IC308
(REAL TIME CLOCK IC)
LED ON : 5V
LED OFF : 0V
(HDLC IC)
IC303
DPNTN
R303 4.7K
LRSTN
SIGN1022
C311 Z0.1µ
C388 1000P
X300 32.768KHZ
C319 20P
C320 20P
2MHZ
LDVD
CENO
TXCEN
CDST1
CDST0
RXCEN
PREOP
TEOP
RST
WD
TRQ
R372 47K
R/WN
HDLCSN
LDSTB
RTCSN
LIORN
LOWRN
R333 47K
LINT2N
LINT1
LINT0N
ROMCSN
R331 47K
CPU IC IC301
100QFP PQV16801JFCG
C316 1000P
C398 Z0.1µ
C399 220P
C3C0 220P
C3A1 220P
C3A2 1000P
CPUCLK
HLTN
RSTN
16.384MHz
R332 47K
R3L5 1.5K
R320 4.7K
R3W0
C308 1000P
X301 32.768KHZ
R327 820
R324 33
R321 0
C305 0
ASN,BAKN,BGTN,BRQN,CPUCLK,DAKN,HLTN,LDSN,LRSTN,R/WN,UDSN
LDSN
R/WN
UDSN
BRQN
BGTN
DAKN
ASN
C309 Z0.1µ
C310 Z0.1µ
R3W2 82
C317 Z0.1µ
C318 Z0.1µ
ASIC
IC IC302
C3A3 15P
C3A4 68P
C3A5 68P
C3A6 68P
C3B0 68P
C3B7 68P
C3B8 68P
C3B9 68P
DRAM IC307
IC305
IC304
IC309
28-SOJ 4M-DRAM
C314
C312
C315
C313
FLASH MEMORY ROM
IC306
FLASH
C321 Z0.1µ
R3L0 0
R3L1 0
R3L2 0
R3L3 0
R3L4 0
R3L5 1.5K
R3L6 0
R3L7 0
R3L8 0
R3L9 0
R3M0 0
R3M1 33
R3M2 33
R3M3 33
R3M4 33
R3M5 33
R3M6 33
R3M7 33
R3M8 33
R3M9 33
R3N0 33
R3N1 33
R3N2 33
R3N3 33
R3N4 33
R3N5 33
R3N6 33
R3N7 33
R3N8 33
R3N9 33
R3P0 0
R3P1 0
R3P2 0
R3P3 0
R3P4 0
R3P5 0
R3P6 0
R3P7 0
R3P8 0
R3P9 0
R3R0 10K
R3R1 10K
R3R2 10K
R3R3 10K
R3R4 10K
R3R5 10K
R3R6 10K
R3R7 10K
R3R8 10K
R3R9 10K
R3S0 10K
R3S1 10K
R3S2 10K
R3S3 10K
R3S4 10K
R3S5 10K
R3S6 10K
R3S7 10K
R3S8 10K
R3S9 10K
R3T0 10K
R3T1 10K
R3T2 10K
R3T3 10K
R3T4 10K
R3T5 10K
R3T6 10K
R3T7 10K
R3T8 10K
R3T9 10K
R3U1 10K
R3U2 10K
R3U3 10K
R3U4 10K
R3U5 10K
R3U6 10K
R3U7 10K
R3U8 10K
R3U9 10K
R3V0 10K
R3V1 10K
R3V2 10K
R3V3 10K
R3V4 10K
R3V5 10K
R3V6 10K
R3V7 10K
R3V8 10K
R3V9 10K
R3W0 10K
R3W1 10K
R3W2 10K
R3W3 10K
R3W4 10K
R3W5 10K
R3W6 10K
R3W7 10K
R3W8 10K
R3W9 10K
R3X0 10K
R3X1 10K
R3X2 10K
R3X3 10K
R3X4 10K
R3X5 10K
R3X6 10K
R3X7 10K
R3X8 10K
R3X9 10K
R3Y0 10K
R3Y1 10K
R3Y2 10K
R3Y3 10K
R3Y4 10K
R3Y5 10K
R3Y6 10K
R3Y7 10K
R3Y8 10K
R3Y9 10K
R3Z0 10K
R3Z1 10K
R3Z2 10K
R3Z3 10K
R3Z4 10K
R3Z5 10K
R3Z6 10K
R3Z7 10K
R3Z8 10K
R3Z9 10K
R3AA0 10K
R3AA1 10K
R3AA2 10K
R3AA3 10K
R3AA4 10K
R3AA5 10K
R3AA6 10K
R3AA7 10K
R3AA8 10K
R3AA9 10K
R3AB0 10K
R3AB1 10K
R3AB2 10K
R3AB3 10K
R3AB4 10K
R3AB5 10K
R3AB6 10K
R3AB7 10K
R3AB8 10K
R3AB9 10K
R3AC0 10K
R3AC1 10K
R3AC2 10K
R3AC3 10K
R3AC4 10K
R3AC5 10K
R3AC6 10K
R3AC7 10K
R3AC8 10K
R3AC9 10K
R3AD0 10K
R3AD1 10K
R3AD2 10K
R3AD3 10K
R3AD4 10K
R3AD5 10K
R3AD6 10K
R3AD7 10K
R3AD8 10K
R3AD9 10K
R3AE0 10K
R3AE1 10K
R3AE2 10K
R3AE3 10K
R3AE4 10K
R3AE5 10K
R3AE6 10K
R3AE7 10K
R3AE8 10K
R3AE9 10K
R3AF0 10K
R3AF1 10K
R3AF2 10K
R3AF3 10K
R3AF4 10K
R3AF5 10K
R3AF6 10K
R3AF7 10K
R3AF8 10K
R3AF9 10K
R3AG0 10K
R3AG1 10K
R3AG2 10K
R3AG3 10K
R3AG4 10K
R3AG5 10K
R3AG6 10K
R3AG7 10K
R3AG8 10K
R3AG9 10K
R3AH0 10K
R3AH1 10K
R3AH2 10K
R3AH3 10K
R3AH4 10K
R3AH5 10K
R3AH6 10K
R3AH7 10K
R3AH8 10K
R3AH9 10K
R3AJ0 10K
R3AJ1 10K
R3AJ2 10K
R3AJ3 10K
R3AJ4 10K
R3AJ5 10K
R3AJ6 10K
R3AJ7 10K
R3AJ8 10K
R3AJ9 10K
R3AK0 10K
R3AK1 10K
R3AK2 10K
R3AK3 10K
R3AK4 10K
R3AK5 10K
R3AK6 10K
R3AK7 10K
R3AK8 10K
R3AK9 10K
R3AL0 10K
R3AL1 10K
R3AL2 10K
R3AL3 10K
R3AL4 10K
R3AL5 10K
R3AL6 10K
R3AL7 10K
R3AL8 10K
R3AL9 10K
R3AM0 10K
R3AM1 10K
R3AM2 10K
R3AM3 10K
R3AM4 10K
R3AM5 10K
R3AM6 10K
R3AM7 10K
R3AM8 10K
R3AM9 10K
R3AN0 10K
R3AN1 10K
R3AN2 10K
R3AN3 10K
R3AN4 10K
R3AN5 10K
R3AN6 10K
R3AN7 10K
R3AN8 10K
R3AN9 10K
R3AP0 10K
R3AP1 10K
R3AP2 10K
R3AP3 10K
R3AP4 10K
R3AP5 10K
R3AP6 10K
R3AP7 10K
R3AP8 10K
R3AP9 10K
R3AR0 10K
R3AR1 10K
R3AR2 10K
R3AR3 10K
R3AR4 10K
R3AR5 10K
R3AR6 10K
R3AR7 10K
R3AR8 10K
R3AR9 10K
R3AS0 10K
R3AS1 10K
R3AS2 10K
R3AS3 10K
R3AS4 10K
R3AS5 10K
R3AS6 10K
R3AS7 10K
R3AS8 10K
R3AS9 10K
R3AT0 10K
R3AT1 10K
R3AT2 10K
R3AT3 10K
R3AT4 10K
R3AT5 10K
R3AT6 10K
R3AT7 10K
R3AT8 10K
R3AT9 10K
R3AU0 10K
R3AU1 10K
R3AU2 10K
R3AU3 10K
R3AU4 10K
R3AU5 10K
R3AU6 10K
R3AU7 10K
R3AU8 10K
R3AU9 10K
R3AV0 10K
R3AV1 10K
R3AV2 10K
R3AV3 10K
R3AV4 10K
R3AV5 10K
R3AV6 10K
R3AV7 10K
R3AV8 10K
R3AV9 10K
R3AW0 10K
R3AW1 10K
R3AW2 10K
R3AW3 10K
R3AW4 10K
R3AW5 10K
R3AW6 10K
R3AW7 10K
R3AW8 10K
R3AW9 10K
R3AX0 10K
R3AX1 10K
R3AX2 10K
R3AX3 10K
R3AX4 10K
R3AX5 10K
R3AX6 10K
R3AX7 10K
R3AX8 10K
R3AX9 10K
R3AY0 10K
R3AY1 10K
R3AY2 10K
R3AY3 10K
R3AY4 10K
R3AY5 10K
R3AY6 10K
R3AY7 10K
R3AY8 10K
R3AY9 10K
R3AZ0 10K
R3AZ1 10K
R3AZ2 10K
R3AZ3 10K
R3AZ4 10K
R3AZ5 10K
R3AZ6 10K
R3AZ7 10K
R3AZ8 10K
R3AZ9 10K
R3BA0 10K
R3BA1 10K
R3BA2 10K
R3BA3 10K
R3BA4 10K
R3BA5 10K
R3BA6 10K
R3BA7 10K
R3BA8 10K
R3BA9 10K
R3BB0 10K
R3BB1 10K
R3BB2 10K
R3BB3 10K
R3BB4 10K
R3BB5 10K
R3BB6 10K
R3BB7 10K
R3BB8 10K
R3BB9 10K
R3BC0 10K
R3BC1 10K
R3BC2 10K
R3BC3 10K
R3BC4 10K
R3BC5 10K
R3BC6 10K
R3BC7 10K
R3BC8 10K
R3BC9 10K
R3BD0 10K
R3BD1 10K
R3BD2 10K
R3BD3 10K
R3BD4 10K
R3BD5 10K
R3BD6 10K
R3BD7 10K
R3BD8 10K
R3BD9 10K
R3BE0 10K
R3BE1 10K
R3BE2 10K
R3BE3 10K
R3BE4 10K
R3BE5 10K
R3BE6 10K
R3BE7 10K
R3BE8 10K
R3BE9 10K
R3BF0 10K
R3BF1 10K
R3BF2 10K
R3BF3 10K
R3BF4 10K
R3BF5 10K
R3BF6 10K
R3BF7 10K
R3BF8 10K
R3BF9 10K
R3BG0 10K
R3BG1 10K
R3BG2 10K
R3BG3 10K
R3BG4 10K
R3BG5 10K
R3BG6 10K
R3BG7 10K
R3BG8 10K
R3BG9 10K
R3BH0 10K
R3BH1 10K
R3BH2 10K
R3BH3 10K
R3BH4 10K
R3BH5 10K
R3BH6 10K
R3BH7 10K
R3BH8 10K
R3BH9 10K
R3BJ0 10K
R3BJ1 10K
R3BJ2 10K
R3BJ3 10K
R3BJ4 10K
R3BJ5 10K
R3BJ6 10K
R3BJ7 10K
R3BJ8 10K
R3BJ9 10K
R3BK0 10K
R3BK1 10K
R3BK2 10K
R3BK3 10K
R3BK4 10K
R3BK5 10K
R3BK6 10K
R3BK7 10K
R3BK8 10K
R3BK9 10K
R3BL0 10K
R3BL1 10K
R3BL2 10K
R3BL3 10K
R3BL4 10K
R3BL5 10K
R3BL6 10K
R3BL7 10K
R3BL8 10K
R3BL9 10K
R3BM0 10K
R3BM1 10K
R3BM2 10K
R3BM3 10K
R3BM4 10K
R3BM5 10K
R3BM6 10K
R3BM7 10K
R3BM8 10K
R3BM9 10K
R3BN0 10K
R3BN1 10K
R3BN2 10K
R3BN3 10K
R3BN4 10K
R3BN5 10K
R3BN6 10K
R3BN7 10K
R3BN8 10K
R3BN9 10K
R3BP0 10K
R3BP1 10K
R3BP2 10K
R3BP3 10K
R3BP4 10K
R3BP5 10K
R3BP6 10K
R3BP7 10K
R3BP8 10K
R3BP9 10K
R3BR0 10K
R3BR1 10K
R3BR2 10K
R3BR3 10K
R3BR4 10K
R3BR5 10K
R3BR6 10K
R3BR7 10K
R3BR8 10K
R3BR9 10K
R3BS0 10K
R3BS1 10K
R3BS2 10K
R3BS3 10K
R3BS4 10K
R3BS5 10K
R3BS6 10K
R3BS7 10K
R3BS8 10K
R3BS9 10K
R3BT0 10K
R3BT1 10K
R3BT2 10K
R3BT3 10K
R3BT4 10K
R3BT5 10K
R3BT6 10K
R3BT7 10K
R3BT8 10K
R3BT9 10K
R3BU0 10K
R3BU1 10K
R3BU2 10K
R3BU3 10K
R3BU4 10K
R3BU5 10K
R3BU6 10K
R3BU7 10K
R3BU8 10K
R3BU9 10K
R3BV0 10K
R3BV1 10K
R3BV2 10K
R3BV3 10K
R3BV4 10K
R3BV5 10K
R3BV6 10K
R3BV7 10K
R3BV8 10K
R3BV9 10K
R3BW0 10K
R3BW1 10K
R3BW2 10K
R3BW3 10K
R3BW4 10K
R3BW5 10K
R3BW6 10K
R3BW7 10K
R3BW8 10K
R3BW9 10K
R3BX0 10K
R3BX1 10K
R3BX2 10K
R3BX3 10K
R3BX4 10K
R3BX5 10K
R3BX6 10K
R3BX7 10K
R3BX8 10K
R3BX9 10K
R3BY0 10K
R3BY1 10K
R3BY2 10K
R3BY3 10K
R3BY4 10K
R3BY5 10K
R3BY6 10K
R3BY7 10K
R3BY8 10K
R3BY9 10K
R3BZ0 10K
R3BZ1 10K
R3BZ2 10K
R3BZ3 10K
R3BZ4 10K
R3BZ5 10K
R3BZ6 10K
R3BZ7 10K
R3BZ8 10K
R3BZ9 10K
R3CA0 10K
R3CA1 10K
R3CA2 10K
R3CA3 10K
R3CA4 10K
R3CA5 10K
R3CA6 10K
R3CA7 10K
R3CA8 10K
R3CA9 10K
R3CB0 10K
R3CB1 10K
R3CB2 10K
R3CB3 10K
R3CB4 10K
R3CB5 10K
R3CB6 10K
R3CB7 10K
R3CB8 10K
R3CB9 10K
R3CC0 10K
R3CC1 10K
R3CC2 10K
R3CC3 10K
R3CC4 10K
R3CC5 10K
R3CC6 10K
R3CC7 10K
R3CC8 10K
R3CC9 10K
R3CD0 10K
R3CD1 10K
R3CD2 10K
R3CD3 10K
R3CD4 10K
R3CD5 10K
R3CD6 10K
R3CD7 10K
R3CD8 10K
R3CD9 10K
R3CE0 10K
R3CE1 10K
R3CE2 10K
R3CE3 10K
R3CE4 10K
R3CE5 10K
R3CE6 10K
R3CE7 10K
R3CE8 10K
R3CE9 10K
R3CF0 10K
R3CF1 10K
R3CF2 10K
R3CF3 10K
R3CF4 10K
R3CF5 10K
R3CF6 10K
R3CF7 10K
R3CF8 10K
R3CF9 10K
R3CG0 10K
R3CG1 10K
R3CG2 10K
R3CG3 10K
R3CG4 10K
R3CG5 10K
R3CG6 10K
R3CG7 10K
R3CG8 10K
R3CG9 10K
R3CH0 10K
R3CH1 10K
R3CH2 10K
R3CH3 10K
R3CH4 10K
R3CH5 10K
R3CH6 10K
R3CH7 10K
R3CH8 10K
R3CH9 10K
R3CJ0 10K
R3CJ1 10K
R3CJ2 10K
R3CJ3 10K
R3CJ4 10K
R3CJ5 10K
R3CJ6 10K
R3CJ7 10K
R3CJ8 10K
R3CJ9 10K
R3CK0 10K
R3CK1 10K
R3CK2 10K
R3CK3 10K
R3CK4 10K
R3CK5 10K
R3CK6 10K
R3CK7 10K
R3CK8 10K
R3CK9 10K
R3CL0 10K
R3CL1 10K
R3CL2 10K
R3CL3 10K
R3CL4 10K
R3CL5 10K
R3CL6 10K
R3CL7 10K
R3CL8 10K
R3CL9 10K
R3CM0 10K
R3CM1 10K
R3CM2 10K
R3CM3 10K
R3CM4 10K
R3CM5 10K
R3CM6 10K
R3CM7 10K
R3CM8 10K
R3CM9 10K
R3CN0 10K
R3CN1 10K
R3CN2 10K
R3CN3 10K
R3CN4 10K
R3CN5 10K
R3CN6 10K
R3CN7 10K
R3CN8 10K
R3CN9 10K
R3CP0 10K
R3CP1 10K
R3CP2 10K
R3CP3 10K
R3CP4 10K
R3CP5 10K
R3CP6 10K
R3CP7 10K
R3CP8 10K
R3CP9 10K
R3CR0 10K
R3CR1 10K
R3CR2 10K
R3CR3 10K
R3CR4 10K
R3CR5 10K
R3CR6 10K
R3CR7 10K
R3CR8 10K
R3CR9 10K
R3CS0 10K
R3CS1 10K
R3CS2 10K
R3CS3 10K
R3CS4 10K
R3CS5 10K
R3CS6 10K
R3CS7 10K
R3CS8 10K
R3CS9 10K
R3CT0 10K
R3CT1 10K
R3CT2 10K
R3CT3 10K
R3CT4 10K
R3CT5 10K
R3CT6 10K
R3CT7 10K
R3CT8 10K
R3CT9 10K
R3CU0 10K
R3CU1 10K
R3CU2 10K
R3CU3 10K
R3CU4 10K
R3CU5 10K
R3CU6 10K
R3CU7 10K
R3CU8 10K
R3CU9 10K
R3CV0 10K
R3CV1 10K
R3CV2 10K
R3CV3 10K
R3CV4 10K
R3CV5 10K
R3CV6 10K
R3CV7 10K
R3CV8 10K
R3CV9 10K
R3CW0 10K
R3CW1 10K
R3CW2 10K
R3CW3 10K
R3CW4 10K
R3CW5 10K
R3CW6 10K
R3CW7 10K
R3CW8 10K
R3CW9 10K
R3CX0 10K
R3CX1 10K
R3CX2 10K
R3CX3 10K
R3CX4 10K
R3CX5 10K
R3CX6 10K
R3CX7 10K
R3CX8 10K
R3CX9 10K
R3CY0 10K
R3CY1 10K
R3CY2 10K
R3CY3 10K
R3CY4 10K
R3CY5 10K
R3CY6 10K
R3CY7 10K
R3CY8 10K
R3CY9 10K
R3CZ0 10K
R3CZ1 10K
R3CZ2 10K
R3CZ3 10K
R3CZ4 10K
R3CZ5 10K
R3CZ6 10K
R3CZ7 10K
R3CZ8 10K
R3CZ9 10K
R3DA0 10K
R3DA1 10K
R3DA2 10K
R3DA3 10K
R3DA4 10K
R3DA5 10K
R3DA6 10K
R3DA7 10K
R3DA8 10K
R3DA9 10K
R3DB0 10K
R3DB1 10K
R3DB2 10K
R3DB3 10K
R3DB4 10K
R3DB5 10K
R3DB6 10K
R3DB7 10K
R3DB8 10K
R3DB9 10K
R3DC0 10K
R3DC1 10K
R3DC2 10K
R3DC3 10K
R3DC4 10K
R3DC5 10K
R3DC6 10K
R3DC7 10K
R3DC8 10K
R3DC9 10K
R3DD0 10K
R3DD1 10K
R3DD2 10K
R3DD3 10K
R3DD4 10K
R3DD5 10K
R3DD6 10K
R3DD7 10K
R3DD8 10K
R3DD9 10K
R3DE0 10K
R3DE1 10K
R3DE2 10K
R3DE3 10K
R3DE4 10K
R3DE5 10K
R3DE6 10K
R3DE7 10K
R3DE8 10K
R3DE9 10K
R3DF0 10K
R3DF1 10K
R3DF2 10K
R3DF3 10K
R3DF4 10K
R3DF5 10K
R3DF6 10K
R3DF7 10K
R3DF8 10K
R3DF9 10K
R3DG0 10K
R3DG1 10K
R3DG2 10K
R3DG3 10K
R3DG4 10K
R3DG5 10K
R3DG6 10K
R3DG7 10K
R3DG8 10K
R3DG9 10K
R3DH0 10K
R3DH1 10K
R3DH2 10K
R3DH3 10K
R3DH4 10K
R3DH5 10K
R3DH6 10K
R3DH7 10K
R3DH8 10K
R3DH9 10K
R3DJ0 10K
R3DJ1 10K
R3DJ2 10K
R3DJ3 10K
R3DJ4 10K
R3DJ5 10K
R3DJ6 10K
R3DJ7 10K
R3DJ8 10K
R3DJ9 10K
R3DK0 10K
R3DK1 10K
R3DK2 10K
R3DK3 10K
R3DK4 10K
R3DK5 10K
R3DK6 10K
R3DK7 10K
R3DK8 10K
R3DK9 10K
R3DL0 10K
R3DL1 10K
R3DL2 10K
R3DL3 10K
R3DL4 10K
R3DL5 10K
R3DL6 10K
R3DL7 10K
R3DL8 10K
R3DL9 10K
R3DM0 10K
R3DM1 10K
R3DM2 10K
R3DM3 10K
R3DM4 10K
R3DM5 10K
R3DM6 10K
R3DM7 10K
R3DM8 10K
R3DM9 10K
R3DN0 10K
R3DN1 10K
R3DN2 10K
R3DN3 10K
R3DN4 10K
R3DN5 10K
R3DN6 10K
R3DN7 10K
R3DN8 10K
R3DN9 10K
R3DP0 10K
R3DP1 10K
R3DP2 10K
R3DP3 10K
R3DP4 10K
R3DP5 10K
R3DP6 10K
R3DP7 10K
R3DP8 10K
R3DP9 10K
R3DR0 10K
R3DR1 10K
R3DR2 10K
R3DR3 10K
R3DR4 10K
R3DR5 10K
R3DR6 10K
R3DR7 10K
R3DR8 10K
R3DR9 10K
R3DS0 10K
R3DS1 10K
R3DS2 10K
R3DS3 10K
R3DS4 10K
R3DS5 10K
R3DS6 10K
R3DS7 10K
R3DS8 10K
R3DS9 10K
R3DT0 10K
R3DT1 10K
R3DT2 10K
R3DT3 10K
R3DT4 10K
R3DT5 10K
R3DT6 10K
R3DT7 10K
R3DT8 10K
R3DT9 10K
R3DU0 10K
R3DU1 10K
R3DU2 10K
R3DU3 10K
R3DU4 10K
R3DU5 10K
R3DU6 10K
R3DU7 10K
R3DU8 10K
R3DU9 10K
R3DV0 10K
R3DV1 10K
R3DV2 10K
R3DV3 10K
R3DV4 10K
R3DV5 10K
R3DV6 10K
R3DV7 10K
R3DV8 10K
R3DV9 10K
R3DW0 10K
R3DW1 10K
R3DW2 10K
R3DW3 10K
R3DW4 10K
R3DW5 10K
R3DW6 10K
R3DW7 10K
R3DW8 10K
R3DW9 10K
R3DX0 10K
R3DX1 10K
R3DX2 10K
R3DX3 10K
R3DX4 10K
R3DX5 10K
R3DX6 10K
R3DX7 10K
R3DX8 10K
R3DX9 10K
R3DY0 10K
R3DY1 10K
R3DY2 10K
R3DY3 10K
R3DY4 10K
R3DY5 10K
R3DY6 10K
R3DY7 10K
R3DY8 10K
R3DY9 10K
R3DZ0 10K
R3DZ1 10K
R3DZ2 10K
R3DZ3 10K
R3DZ4 10K
R3DZ5 10K
R3DZ6 10K
R3DZ7 10K
R3DZ8 10K
R3DZ9 10K
R3EA0 10K
R3EA1 10K
R3EA2 10K
R3EA3 10K
R3EA4 10K
R3EA5 10K
R3EA6 10K
R3EA7 10K
R3EA8 10K
R3EA9 10K
R3EB0 10K
R3EB1 10K
R3EB2 10K
R3EB3 10K
R3EB4 10K
R3EB5 10K
R3EB6 10K
R3EB7 10K
R3EB8 10K
R3EB9 10K
R3EC0 10K
R3EC1 10K
R3EC2 10K
R3EC3 10K
R3EC4 10K
R3EC5 10K
R3EC6 10K
R3EC7 10K
R3EC8 10K
R3EC9 10K
R3ED0 10K
R3ED1 10K
R3ED2 10K
R3ED3 10K
R3ED4 10K
R3ED5 10K
R3ED6 10K
R3ED7 10K
R3ED8 10K
R3ED9 10K
R3EE0 10K
R3EE1 10K
R3EE2 10K
R3EE3 10K
R3EE4 10K
R3EE5 10K
R3EE6 10K
R3EE7 10K
R3EE8 10K
R3EE9 10K
R3EF0 10K
R3EF1 10K
R3EF2 10K
R3EF3 10K
R3EF4 10K
R3EF5 10K
R3EF6 10K
R3EF7 10K
R3EF8 10K
R3EF9 10K
R3EG0 10K
R3EG1 10K
R3EG2 10K
R3EG3 10K
R3EG4 10K
R3EG5 10K
R3EG6 10K
R3EG7 10K
R3EG8 10K
R3EG9 10K
R3EH0 10K
R3EH1 10K
R3EH2 10K
R3EH3 10K
R3EH4 10K
R3EH5 10K
R3EH6 10K
R3EH7 10K
R3EH8 10K
R3EH9 10K
R3EJ0 10K
R3EJ1 10K
R3EJ2 10K
R3EJ3 10K
R3EJ4 10K
R3EJ5 10K
R3EJ6 10K
R3EJ7 10K
R3EJ8 10K
R3EJ9 10K
R3EK0 10K
R3EK1 10K
R3EK2 10K
R3EK3 10K
R3EK4 10K
R3EK5 10K
R3EK6 10K
R3EK7 10K
R3EK8 10K
R3EK9 10K
R3EL0 10K
R3EL1 10K
R3EL2 10K
R3EL3 10K
R3EL4 10K
R3EL5 10K
R3EL6 10K
R3EL7 10K
R3EL8 10K
R3EL9 10K
R3EM0 10K
R3EM1 10K
R3EM2 10K
R3EM3 10K
R3EM4 10K
R3EM5 10K
R3EM6 10K
R3EM7 10K
R3EM8 10K
R3EM9 10K
R3EN0 10K
R3EN1 10K
R3EN2 10K
R3EN3 10K
R3EN4 10K
R3EN5 10K
R3EN6 10K
R3EN7 10K
R3EN8 10K
R3EN9 10K
R3EP0 10K
R3EP1 10K
R3EP2 10K
R3EP3 10K
R3EP4 10K
R3EP5 10K
R3EP6 10K
R3EP7 10K
R3EP8 10K
R3EP9 10K
R3ER0 10K
R3ER1 10K
R3ER2 10K
R3ER3 10K
R3ER4 10K
R3ER5 10K
R3ER6 10K
R3ER7 10K
R3ER8 10K
R3ER9 10K
R3ES0 10K
R3ES1 10K
R3ES2 10K
R3ES3 10K
R3ES4 10K
R3ES5 10K
R3ES6 10K
R3ES7 10K
R3ES8 10K
R3ES9 10K
R3ET0 10K
R3ET1 10K
R3ET2 10K
R3ET3 10K
R3ET4 10K
R3ET5 10K
R3ET6 10K
R3ET7 10K
R3ET8 10K
R3ET9 10K
R3EU0 10K
R3EU1 10K
R3EU2 10K
R3EU3 10K
R3EU4 10K
R3EU5 10K
R3EU6 10K
R3EU7 10K
R3EU8 10K
R3EU9 10K
R3EV0 10K
R3EV1 10K
R3EV2 10K
R3EV3 10K
R3EV4 10K
R3EV5 10K
R3EV6 10K
R3EV7 10K
R3EV8 10K
R3EV9 10K
R3EW0 10K
R3EW1 10K
R3EW2 10K
R3EW3 10K
R3EW4 10K
R3EW5 10K
R3EW6 10K
R3EW7 10K
R3EW8 10K
R3EW9 10K
R3EX0 10K
R3EX1 10K
R3EX2 10K
R3EX3 10K
R3EX4 10K
R3EX5 10K
R3EX6 10K
R3EX7 10K
R3EX8 10K
R3EX9 10K
R3EY0 10K
R3EY1 10K
R3EY2 10K
R3EY3 10K
R3EY4 10K
R3EY5 10K
R3EY6 10K
R3EY7 10K
R3EY8 10K
R3EY9 10K
R3EZ0 10K
R3EZ1 10K
R3EZ2 10K
R3EZ3 10K
R3EZ4 10K
R3EZ5 10K
R3EZ6 10K
R3EZ7 10K
R3EZ8 10K
R3EZ9 10K
R3FA0 10K
R3FA1 10K
R3FA2 10K
R3FA3 10K
R3FA4 10K
R3FA5 10K
R3FA6 10K
R3FA7 10K
R3FA8 10K
R3FA9 10K
R3FB0 10K
R3FB1 10K
R3FB2 10K
R3FB3 10K
R3FB4 10K
R3FB5 10K
R3FB6 10K
R3FB7 10K
R3FB8 10K
R3FB9 10K
R3FC0 10K
R3FC1 10K
R3FC2 10K
R3FC3 10K
R3FC4 10K
R3FC5 10K
R3FC6 10K
R3FC7 10K
R3FC8 10K
R3FC9 10K
R3FD0 10K
R3FD1 10K
R3FD2 10K
R3FD3 10K
R3FD4 10K
R3FD5 10K
R3FD6 10K
R3FD7 10K
R3FD8 10K
R3FD9 10K
R3FE0 10K
R3FE1 10K
R3FE2 10K
R3FE3 10K
R3FE4 10K
R3FE5 10K
R3FE6 10K
R3FE7 10K
R3FE8 10K
R3FE9 10K
R3FF0 10K
R3FF1 10K
R3FF2 10K
R3FF3 10K
R3FF4 10K
R3FF5 10K
R3FF6 10K
R3FF7 10K
R3FF8 10K
R3FF9 10K
R3FG0 10K
R3FG1 10K
R3FG2 10K
R3FG3 10K
R3FG4 10K
R3FG5 10K
R3FG6 10K
R3FG7 10K
R3FG8 10K
R3FG9 10K
R3FH0 10K
R3FH1 10K
R3FH2 10K
R3FH3 10K
R3FH4 10K
R3FH5 10K
R3FH6 10K
R3FH7 10K
R3FH8 10K
R3FH9 10K
R3FJ0 10K
R3FJ1 10K
R3FJ2 10K
R3FJ3 10K
R3FJ4 10K
R3FJ5 10K
R3FJ6 10K
R3FJ7 10K
R3FJ8 10K
R3FJ9 10K
R3FK0 10K
R3FK1 10K
R3FK2 10K
R3FK3 10K
R3FK4 10K
R3FK5 10K
R3FK6 10K
R3FK7 10K
R3FK8 10K
R3FK9 10K
R3FL0 10K
R3FL1 10K
R3FL2 10K
R3FL3 10K
R3FL4 10K
R3FL5 10K
R3FL6 10K
R3FL7 10K
R3FL8 10K
R3FL9 10K
R3FM0 10K
R3FM1 10K
R3FM2 10K
R3FM3 10K
R3FM4 10K
R3FM5 10K
R3FM6 10K
R3FM7 10K
R3FM8 10K
R3FM9 10K
R3FN0 10K
R3FN1 10K
R3FN2 10K
R3FN3 10K
R3FN4 10K
R3FN5 10K
R3FN6 10K
R3FN7 10K
R3FN8 10K
R3FN9 10K
R3FP0 10K
R3FP1 10K
R3FP2 10K
R3FP3 10K
R3FP4 10K
R3FP5 10K
R3FP6 10K
R3FP7 10K
R3FP8 10K
R3FP9 10K
R3FR0 10K
R3FR1 10K
R3FR2 10K
R3FR3 10K
R3FR4 10K
R3FR5 10K
R3FR6 10K
R3FR7 10K
R3FR8 10K
R3FR9 10K
R3FS0 10K
R3FS1 10K
R3FS2 10K
R3FS3 10K
R3FS4 10K
R3FS5 10K
R3FS6 10K
R3FS7 10K
R3FS8 10K
R3FS9 10K
R3FT0 10K
R3FT1 10K
R3FT2 10K
R3FT3 10K
R3FT4 10K
R3FT5 10K
R3FT6 10K
R3FT7 10K
R3FT8 10K
R3FT9 10K
R3FU0 10K
R3FU1 10K
R3FU2 10K
R3FU3 10K
R3FU4 10K
R3FU5 10K
R3FU6 10K
R3FU7 10K
R3FU8 10K
R3FU9 10K
R3FV0 10K
R3FV1 10K
R3FV2 10K
R3FV3 10K
R3FV4 10K
R3FV5 10K
R3FV6 10K
R3FV7 10K
R3FV8 10K
R3FV9 10K
R3FW0 10K
R3FW1 10K
R3FW2 10K
R3FW3 10K
R3FW4 10K
R3FW5 10K
R3FW6 10K
R3FW7 10K
R3FW8 10K
R3FW9 10K
R3FX0 10K
R3FX1 10K
R3FX2 10K
R3FX3 10K
R3FX4 10K
R3FX5 10K
R3FX6 10K
R3FX7 10K
R3FX8 10K
R3FX9 10K
R3FY0 10K
R3FY1 10K
R3FY2 10K
R3FY3 10K
R3FY4 10K
R3FY5 10K
R3FY6 10K
R3FY7 10K
R3FY8 10K
R3FY9 10K
R3FZ0 10K
R3FZ1 10K
R3FZ2 10K
R3FZ3 10K
R3FZ4 10K
R3FZ5 10K
R3FZ6 10K
R3FZ7 10K
R3FZ8 10K
R3FZ9 10K
R3GA0 10K
R3GA1 10K
R3GA2 10K
R3GA3 10K
R3GA4 10K
R3GA5 10K
R3GA6 10K
R3GA7 10K
R3GA8 10K
R3GA9 10K
R3GB0 10K
R3GB1 10K
R3GB2 10K
R3GB3 10K
R3GB4 10K
R3GB5 10K
R3GB6 10K
R3GB7 10K
R3GB8 10K
R3GB9 10K
R3GC0 10K
R3GC1 10K
R3GC2 10K
R3GC3 10K
R3GC4 10K
R3GC5 10K
R3GC6 10K
R3GC7 10K
R3GC8 10K
R3GC9 10K
R3GD0 10K
R3GD1 10K
R3GD2 10K
R3GD3 10K
R3GD4 10K
R3GD5 10K
R3GD6 10K
R3GD7 10K
R3GD8 10K
R3GD9 10K
R3GE0 10K
R3GE1 10K
R3GE2 10K
R3GE3 10K
R3GE4 10K
R3GE5 10K
R3GE6 10K
R3GE7 10K
R3GE8 10K
R3GE9 10K
R3GF0 10K
R3GF1 10K
R3GF2 10K
R3GF3 10K
R3GF4 10K
R3GF5 10K
R3GF6 10K
R3GF7 10K
R3GF8 10K
R3GF9 10K
R3GG0 10K
R3GG1 10K
R3GG2 10K
R3GG3 10K
R3GG4 10K
R3GG5 10K
R3GG6 10K
R3GG7 10K
R3GG8 10K
R3GG9 10K
R3GH0 10K
R3GH1 10K
R3GH2 10K
R3GH3 10K
R3GH4 10K
R3GH5 10K
R3GH6 10K
R3GH7 10K
R3GH8 10K
R3GH9 10K
R3GJ0 10K
R3GJ1 10K
R3GJ2 10K
R3GJ3 10K
R3GJ4 10

KX-TVS120 MAIN BOARD No.2


KX-TVS120 DPT INTERFACE CARD(KX-TVS204) No.1
CN101
HOST I/F (50P)
144-FQFP
IC101B COL-ASIC (CH3, CH4)
IC102 LS244
IC103 LS244
IC104 LS245
IC105 LS241
IC106A
IC106B
IC107
IC108
VDD
-5VA
+5VA
SA01
SA02
SA03
SA04
SA05
SA06
ESA0
ESA1
ESA2
SCSN
SDSTBN
SR/WN
SD0
SD1
SD2
SD3
SD4
SD5
SD6
SD7
SDENNB
SDENNA
SDEN
SL1
SL2
RSTN
SYNCN
4MHZ
LUVDNB
LUVANB
LUVCNB
LDVCN
LDVDN
VHWENNB
PHWENNB
INT0B
MODE1B
LUVDNA
LUVANA
LUVCNA
VHWENNA
DVCN
DVDN
DPDN
UPDN
LINTN
LDVCN
LDVDN
PHWENNB
INT0B
DSPCLK
DCLK
LDSAN
LR/WAN
LSTBAN
LRSTAN
LAA0
LAA1
LAA2
LAA11
LAA12
LAA13
LAA14
LAA15
LAB0
LAB1
LAB2
LAB11
LAB12
LAB13
LAB14
LAB15
DIR=0 : B->A
1 : A->B
(1)
(2)
(3)
(4)
(5)
(6)
(7)
(8)
(9)
(10)
(11)
(12)
(13)
(14)
(15)
(16)
(17)
(18)
(19)
(20)
(21)
(22)
(23)
(24)
(25)
(26)
(27)
(28)
(29)
(30)
(31)
(32)
(33)
(34)
(35)
(36)
(37)
(38)
(39)
(40)
(41)
(42)


(1) (2) (3) (4) (5) (6) (7) (8) (9) (10) (11) (12) (13) (14) (15) (16) (17) (18) (19) (20) (21)(22)(23)(24)(25)(26)(27)(28) (29)(30)(31)(32)(33)(34)(35)(36)(37)(38)(39)(40)(41) (42)
IC109C 100-QFP DSP LSI (CH3)
IC109D 100-QFP DSP LSI (CH4)
FAX I/F (60P) CN102
VDD
-5V
DTXC
DRXD
DRXC
DTXD
DSPCLK
CLK1C
CLK2C
CLK1D
CLK2D
MP/MCN
LRSTBN
LR/WBN
LSTBBN
LDSBN
LDSAN
CCK1
CDE-X
CDE-Y
DPD
UPD
MODE1B
DTXA
DTXB
DRXA
DRXB
DTAC
DTAD
DRAC
DRAD
DRAA
DRAB
4MHZ
SYNC
RST
INT
RWN
STD
TOST
ESA0
ESA1
ESA2
N.C.
SL1
SL2
KX-TVS120 DPT INTERFACE CARD(KX-TVS204) No.2